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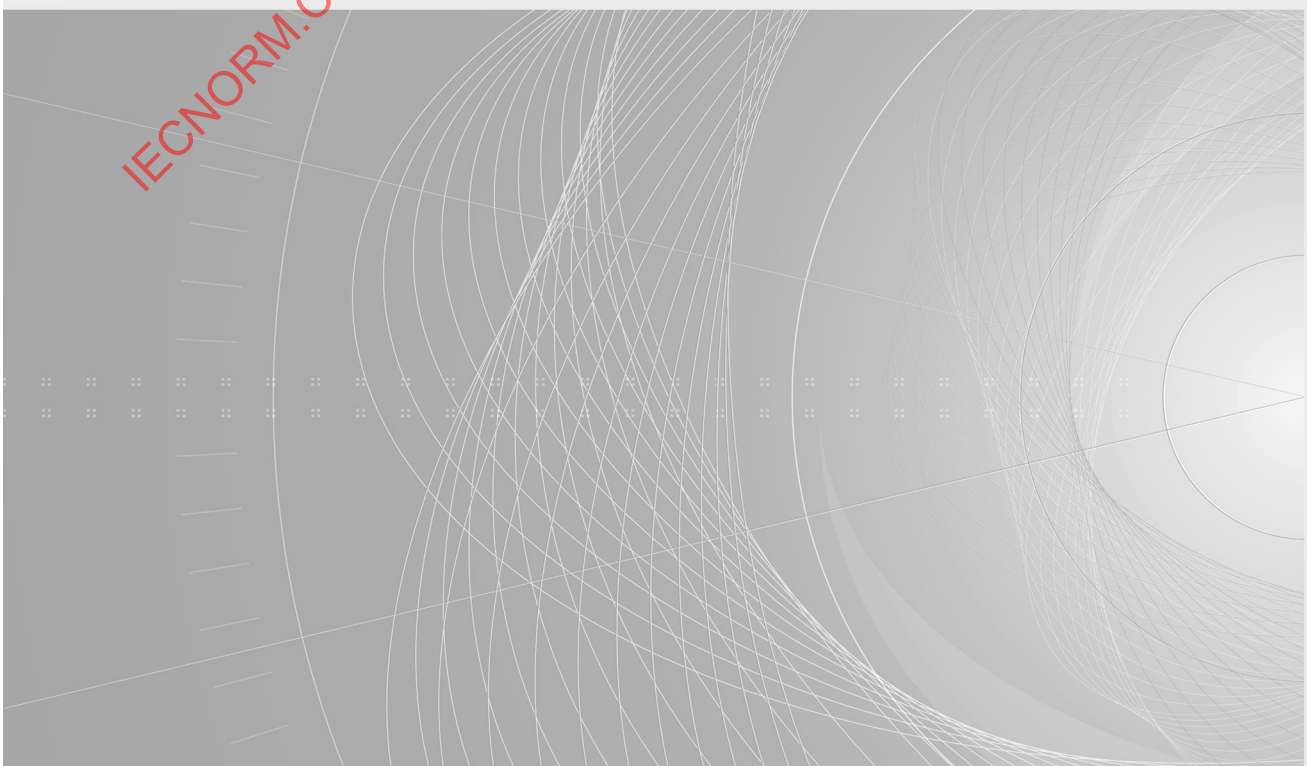
REDLINE VERSION

INTERNATIONAL STANDARD

Semiconductor devices – Mechanical and climatic test methods – Part 28: Electrostatic discharge (ESD) sensitivity testing – Charged device model (CDM) – device level



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colour inside

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CONTENTS

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SEMICONDUCTOR DEVICES – MECHANICAL AND CLIMATIC TEST METHODS –

Part 28: Electrostatic discharge (ESD) sensitivity testing – Charged device model (CDM) – device level

FOREWORD

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This redline version of the official IEC Standard allows the user to identify the changes made to the previous edition IEC 60749-28:2017. A vertical bar appears in the margin wherever a change has been made. Additions are in green text, deletions are in strikethrough red text.

IEC 60749-28 has been prepared by IEC technical committee 47: Semiconductor devices, in collaboration with IEC technical committee 101: Electrostatics. It is an International Standard.

ANSI/ESDA/JEDEC JS-002-2018 has served as a basis for the elaboration of this standard. It is used with permission of the copyright holders, ESD Association and JEDEC Solid state Technology Association. ANSI/ESDA/JEDEC JS-002-2018 describes the field-induced (FI) method. An alternative, the direct contact (DC) method (not based on JS-002-2018), is described in Annex J.

This second edition cancels and replaces the first edition published in 2017. This edition constitutes a technical revision.

This edition includes the following significant technical changes with respect to the previous edition:

a) a new subclause and annex relating to the problems associated with CDM testing of integrated circuits and discrete semiconductors in very small packages;
b) changes to clarify cleaning of devices and testers.

The text of this International Standard is based on the following documents:

Draft	Report on voting
47/2746/FDIS	47/2754/RVD

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/standardsdev/publications.

A list of all parts in the IEC 60749 series, published under the general title *Semiconductor devices – Mechanical and climatic test methods*, can be found on the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

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INTRODUCTION

The earliest electrostatic discharge (ESD) test models and standards simulate a charged object approaching a device and discharging through the device. The most common example is IEC 60749-26, the human body model (HBM). However, with the increasing use of automated device handling systems, another potentially destructive discharge mechanism, the charged device model (CDM), becomes increasingly important. In the CDM, a device itself becomes charged (e.g. by sliding on a surface (tribocharging) or by electric field induction) and is rapidly discharged (by an ESD event) as it closely approaches a conductive object. A critical feature of the CDM is the metal-metal discharge, which results in a very rapid transfer of charge through an air breakdown arc. The CDM test method also simulates metal-metal discharges arising from other similar scenarios, such as the discharging of charged metal objects to devices at different potential.

Accurately quantifying and reproducing this fast metal-metal discharge event is very difficult, if not impossible, due to the limitations of the measuring equipment and its influence on the discharge event. The CDM discharge is generally completed in a few nanoseconds, and peak currents of tens of amperes have been observed. The peak current into the device will vary considerably depending on a large number of factors, including package type and parasitics. The typical failure mechanism observed in MOS devices for the CDM model is dielectric damage, although other damage has been noted.

The CDM charge voltage sensitivity of a given device is package dependent. For example, the same integrated circuit (IC) in a small area package can be less susceptible to CDM damage at a given voltage compared to that same IC in a package of the same type with a larger area. It has been shown that CDM damage susceptibility correlates better to peak current levels than charge voltage.

SEMICONDUCTOR DEVICES – MECHANICAL AND CLIMATIC TEST METHODS –

Part 28: Electrostatic discharge (ESD) sensitivity testing – Charged device model (CDM) – device level

1 Scope

This part of IEC 60749 establishes the procedure for testing, evaluating, and classifying devices and microcircuits according to their susceptibility (sensitivity) to damage or degradation by exposure to a defined field-induced charged device model (CDM) electrostatic discharge (ESD). All packaged semiconductor devices, thin film circuits, surface acoustic wave (SAW) devices, opto-electronic devices, hybrid integrated circuits (HICs), and multi-chip modules (MCMs) containing any of these devices are to be evaluated according to this document. To perform the tests, the devices are assembled into a package similar to that expected in the final application. This CDM document does not apply to socketed discharge model testers. This document describes the field-induced (FI) method. An alternative, the direct contact (DC) method, is described in Annex J.

The purpose of this document is to establish a test method that will replicate CDM failures and provide reliable, repeatable CDM ESD test results from tester to tester, regardless of device type. Repeatable data will allow accurate classifications and comparisons of CDM ESD sensitivity levels.

2 Normative references

There are no normative references in this document.

3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at http://www.electropedia.org/
- ISO Online browsing platform: available at http://www.iso.org/obp

3.1
CDM ESD
charged device model electrostatic discharge
electrostatic discharge (ESD) using the charged device model (CDM) to simulate the actual discharge event that occurs when a charged device is quickly discharged to another object at a lower electrostatic potential through a single pin or terminal

3.2
CDM ESD tester
charged device model electrostatic discharge tester
equipment that simulates the device level CDM ESD event using the non-socketed test method

Note 1 to entry: "Equipment" is referred to as "tester" in this document.

3.3
C_{Small}
device to CDM field plate capacitance for an integrated circuit or discrete semiconductor at or below which it has been determined that CDM testing is not required if specified conditions are met

3.4
dielectric layer
thin insulator placed atop the field plate used to separate the device from the field plate

3.5
field plate
conductive plate used to elevate the potential of the device under test (DUT) by capacitive coupling

Note 1 to entry: See Figure 1.

3.6
ground plane
conductive plate used to complete the circuitry for grounding/discharging the DUT

Note 1 to entry: See Figure 1.

3.7
software voltage
user/operator-entered voltage that, when combined with the scale factor or offset, sets the actual field plate voltage on the system in order to achieve the waveform parameters

Note 1 to entry: Waveform parameters are defined in Table 1 or Table 2.

3.8
test condition
TC
tester plate voltage that meets the waveform parameter conditions

Note 1 to entry: The waveform parameter conditions are found in a particular column of Table 1 and Table 2.

4 Required equipment

4.1 CDM ESD tester

4.1.1 General

Figure 1 represents the hardware schematic for a CDM tester setup to conduct field-induced CDM ESD testing assuming the use of a resistive current probe. The DUT may be an actual device or it may be one of the two verification modules (metal discs) described in Annex A. The pogo pin shall be connected to the ground plane with a 1 Ω current path with a minimum bandwidth (BW) of 9 gigahertz (GHz). The 1 Ω pogo pin to ground connection of the resistive current sensor may be a parallel combination of a 1 Ω resistor between the pogo pin and the ground plane, and the 50 Ω impedance of the oscilloscope and its coaxial cable. In Figure 1, K1 is the switch between charging the field plate and grounding the field plate. The CDM ESD testers used within the context of this document shall meet the waveform characteristics specified in Figure 2, and Table 1 and Table 2, without additional passive or active devices, such as ferrites, in the probe's assembly.

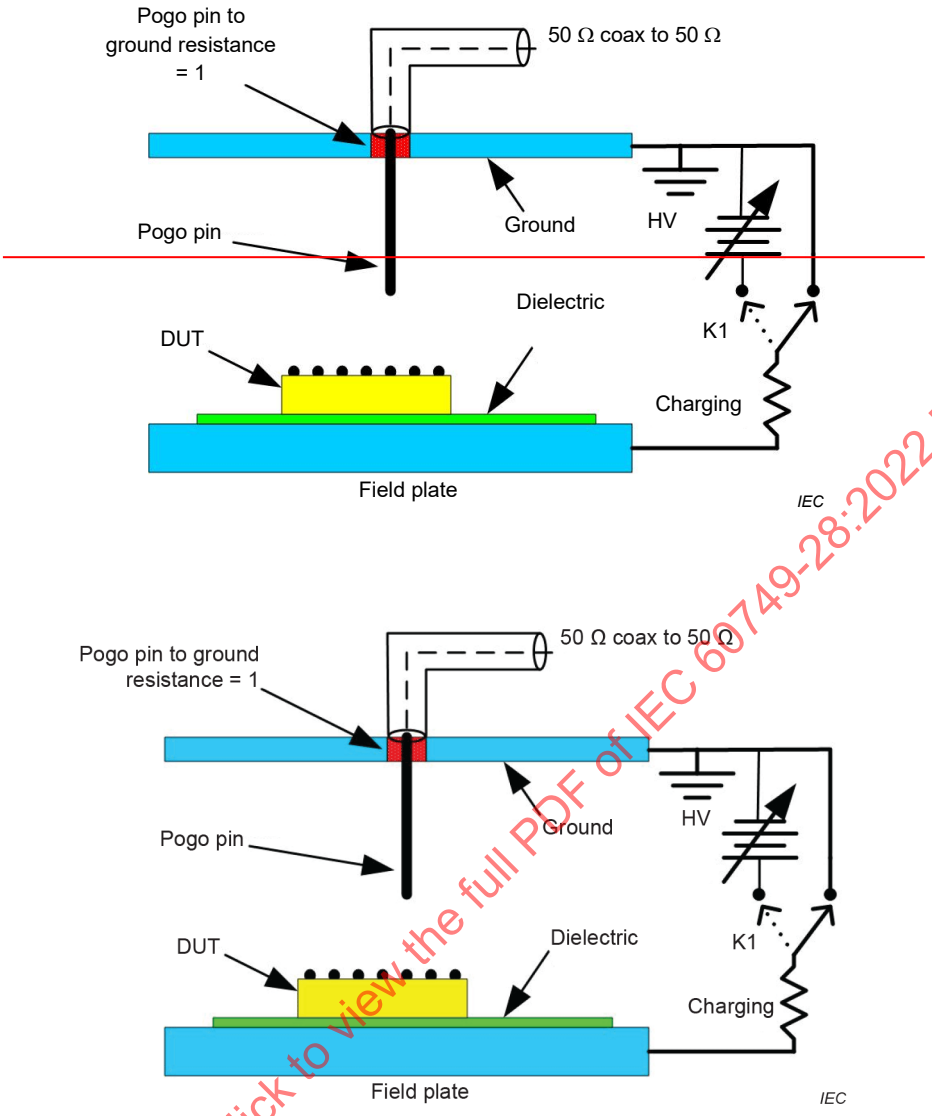


Figure 1 – Simplified CDM tester hardware schematic

When constructing the test equipment, the parasitics in the charge and discharge paths should be minimized since the resistance inductance-capacitance (RLC) parasitics in the equipment greatly influence the test results.

For existing equipment, it is recommended to contact qualified service personnel to determine compliance to this document upon removal of ferrite components.

4.1.2 Current-sensing element

A current-sensing element shall be incorporated into the ground plane. The resistance of this element shall have a value of (1,0 ± 10 %) Ω. A resistor, as specified in 4.1.1, shall be used as the current-sensing element. The value of resistance (including the 50 Ω cable/oscilloscope termination) shall be measured using an ohmmeter as described in 4.5. The resistance value shall be used to calculate the first peak current.

The current-sensing element shall have a minimum frequency response of 9 GHz (specified by a maximum roll-off of 3 dB at 9 GHz).

4.1.3 Ground plane

The probe assembly shall contain a square ground plane with the probe pin centred within it as shown in Figure 1. The dimensions of the ground plane shall be 63,5 mm × 63,5 mm ± 6,35 mm (2,5 inches × 2,5 inches ± 0,25 inches).

4.1.4 Field plate/field plate dielectric layer

The field plate shall have a surface flatness to vary no more than ± 0,127 mm (0,005 inches). The field plate dielectric layer should be made with an FR4 or similar epoxy-glass material. For FR4, the thickness and thickness tolerance of this dielectric layer should be 0,381 mm ± 0,0254 mm (0,015 inches ± 0,001 inches) in order to result in a capacitance measurement (as specified in normative Annex B) in the range specified in Table A.1.

If a different material is used, the material thickness is chosen to result in a capacitance measurement in the range specified in Table A.1.

4.1.5 Charging resistor

The charging resistor shown in Figure 1 shall nominally be 100 MΩ or greater.

Resistor values higher than 100 MΩ may be used, but this may not allow very large devices (refer to 5.9 and Annex I) to charge fully before being discharged by the probe assembly. This effect can be overcome by adding a delay between discharges in the CDM tester programming software. If using a resistor greater than 100 MΩ, it is recommended that the tester or the device itself be characterized to determine if a delay is needed for discharging large devices. A procedure for this large device delay characterization is given in Annex I.

4.2 Waveform measurement equipment

4.2.1 General

The CDM waveform measurement equipment shall consist of the following components.

4.2.2 Cable assemblies

Cable assemblies with combined internal tester cable and external cable total loss of no more than 2 dB at frequencies up to ~~9~~ 5 GHz and a nominal 50 Ω impedance.

4.2.3 Equipment for high-bandwidth waveform measurement

4.2.3.1 High-bandwidth oscilloscope

An oscilloscope or transient digitizer with a minimum real-time (single shot) 3 dB BW of at least 6 GHz and ≥ 20 gigasample/s sampling rate with a nominal 50 Ω input impedance.

4.2.3.2 Attenuator

A 20 dB attenuator with a precision of ±0,5 dB, at least 12 GHz BW, and an impedance of 50 Ω ± 5,0 Ω.

4.2.4 Equipment for 1,0 GHz waveform measurement

4.2.4.1 1 GHz oscilloscope

An oscilloscope or transient digitizer with a real-time (single shot) 3 dB BW of 1 GHz with a nominal 50 Ω input impedance. The sampling rate shall be ≥ 5 gigasample/s.

NOTE The user has the option of using a higher BW oscilloscope and using a hardware or software filter to produce a bandwidth and sampling rate equivalent to that specified in 4.2.4.1.

4.2.4.2 Attenuator

A 20 dB attenuator with a precision of ± 0,5 dB, at least 4 GHz BW, and an impedance of 50 Ω ± 5 Ω.

4.3 Verification modules (metal discs)

The large verification module shall have a capacitance of (55 ± 5 %) pF and the small verification module shall have a capacitance of (6,8 ± 5 %) pF. Refer to normative Annex A for information on the verification module physical dimensions and normative Annex B for information on the capacitance measurement procedure.

4.4 Capacitance meter

Capacitance meter with a resolution of 0,2 pF, a measurement accuracy of 3 %, and a measurement frequency of 1,0 MHz as described in normative Annex B.

4.5 Ohmmeter

The ohmmeter used to measure the resistance of the resistive probe shall be capable of measuring to an accuracy of 0,01 Ω. Use of Kelvin 4-wire connections is recommended.

5 Periodic tester qualification, waveform records, and waveform verification requirements

5.1 Overview of required CDM tester evaluations

The CDM tester shall be qualified, re-qualified, and periodically verified as described in 5.5 and 5.6.

NOTE 1 Dielectric layers, ground planes (ground plates), the coaxial discharging resistor (probe), the distance between the ground plane and the field plate, the verification modules and the discharge contacts (e.g., pogo pins) are key elements of the tester construction. Any change to these elements ~~requires~~ necessitates a waveform verification.

NOTE 2 Changes in the shape of the discharge pulse, even though they can still be within specification, can indicate degradation of the discharge path.

5.2 Waveform capture hardware

Waveform capture requires the following instrumentation and tester set voltage procedure:

- an oscilloscope as specified in 4.2;
- an attenuator and cable assembly as defined in 4.2;
- verification modules (as described in 4.3) with the dimensions and attributes listed in normative Annex A and the method of measurement listed in normative Annex B.

5.3 Waveform capture setup

The waveform capture setup shall be carried out as follows:

a) Clean the verification modules. Avoid skin contact with the modules prior to, and during testing. A recommended procedure is described in normative Annex A.

b) Using an alcohol wipe, clean the discharge probe and the field charge plate on which the device is placed to remove any surface contamination that could result in charge loss. Ensure the pogo pin is free of particulates.

c) Attach the appropriate 20 dB attenuator as described in 4.2.3.2 to the oscilloscope. Attach one end of the external cable assembly, as described in 4.2.2, to the attenuator and the other end to the CDM tester. Verify all connections in the measurement chain are tight.

See informative Annex F for an example of oscilloscope settings and captured waveforms.

5.4 Waveform capture procedure

The waveform capture procedure shall be carried out as follows:

a) Place the verification module to be used on the field plate dielectric, ensuring intimate contact between the field plate dielectric and verification module.

b) Set the potential of the field plate to the needed voltage for the test condition being run.

c) Align the ground pin to approximately the centre of the verification module.

d) Either the single discharge or dual discharge method as described in Clause G.2 or Clause G.3 respectively can be used, but the discharge method chosen should be consistent with how products will be tested. When using the dual discharge method, waveforms for positive and negative pulses require a change in the oscilloscope trigger conditions to capture only positive or negative pulses.

e) Discharge the verification module at least ten times at the polarity being verified.

f) Observe at least ten successive waveforms during the set of discharges above and record the average waveform parameters for I_p, T_r, full width at half maximum (FWHM), and Ip2 for this group of waveforms as shown in Figure 2.

g) If the waveform characteristics do not meet the requirements as defined in either Table 1 or Table 2 for the target test condition (see 5.6 and 5.7 for the appropriate table and test conditions to use), re-clean the verification modules and ground pin, check that all connections are tight, make adjustments in the field plate voltage and repeat steps a) to g).

If this still does not work, check the system vacuum or look at replacement of the ground pin. Consult the tester manufacturer for more information.

Repeat the procedure for the opposite polarity.

5.5 CDM tester qualification/requalification procedure

5.5.1 CDM tester qualification/requalification procedure

The intent of the qualification/requalification procedure is to determine the field plate voltage needed for each test condition setting (125 to 1000) in Table 3 to produce peak current in the ranges corresponding to ~~Table 1 and~~ Table 2, and therefore corresponding to the classification levels as specified in Table 3.

Two alternative procedures for how to qualify and routinely check the CDM test system are introduced in Annex H. These procedures are based on generally available CDM test systems and offer two methods for adjusting the field plate voltage to meet the waveform parameters of ~~Table 1 or~~ Table 2.

CDM test system manufacturers, or test system operators, may develop alternate qualification procedures from the two procedures in Annex H, as long as they result in waveforms that meet the requirements of ~~Table 1 or~~ Table 2 for the various test conditions.

It is recommended that settings determined from this qualification procedure be recorded for a particular test system, oscilloscope BW and polarity. This allows for detection of drift over time on the system, which may indicate a larger issue with the system. See Clause H.3 for examples.

Perform the setup and waveform capture steps as described in 5.3 and 5.5 under test conditions 125 to 1000 in Table 2 for both positive and negative polarities using both small and large verification modules, and measuring with the high bandwidth oscilloscope as specified in 4.2.3.1. Refer to Annex H for example flowcharts of the procedures.

If local site test voltage ranges will always be narrower than the range above (for example test conditions 125 to 500), it is permissible to perform the qualification within that narrower range.

5.5.2 Conditions requiring CDM tester qualification/requalification

The CDM tester qualification and requalification as described in 5.5 is required in the following situations:

- acceptance testing when the CDM tester is delivered; usually performed by the manufacturer during installation;
- periodic requalification in accordance with the manufacturer's recommendations; the maximum time between requalification tests is one year;
- after service or repair that could affect the waveform.

5.5.3 1 GHz oscilloscope correlation with high bandwidth oscilloscope

During the first acceptance testing, the tester manufacturer shall use a high bandwidth oscilloscope as specified in 4.2.3.1 for initial waveform capture. If the test site only has a 1 GHz oscilloscope as specified in 4.2.4.1, the tester manufacturer and end user shall confirm using appropriate bandwidth filtering techniques and comparison with the oscilloscope from the tester manufacturer that the user's oscilloscope measures tester waveforms as defined in Table 1 for quarterly and routine waveform acceptance.

NOTE The Bessel-Thomson software filter option on many oscilloscopes is a ~~recommended~~ suitable high-bandwidth waveform filter as it aligns well with actual 1 GHz oscilloscope data.

Oscilloscope correlation verification shall be repeated if the test site changes 1 GHz oscilloscopes.

5.6 CDM tester quarterly and routine waveform verification procedure

5.6.1 Quarterly waveform verification procedure

Perform the setup and waveform capture steps as described in 5.3 and 5.5 under test conditions 125 to 1 000 in Table 1 using the 1 GHz oscilloscope as specified in 4.2.4.1 or Table 2 using the high-bandwidth oscilloscope as specified in 4.2.3.1. Both verification modules shall be checked at positive and negative polarities. Recommendation is to use the high bandwidth oscilloscope if the option exists. Refer to Annex H for example flowcharts of the procedures.

If local site test voltage ranges will always be narrower than the range above (for example test conditions 125 to 500), it is permissible to perform the qualification within that narrower range.

Tester waveform verification shall be performed at least once per quarter.

5.6.2 Routine waveform verification procedure

5.6.2.1 General

Perform the setup and waveform capture steps as described in 5.3 and 5.5 under test condition 500 in Table 1 (1 GHz oscilloscope) or Table 2 (high-bandwidth oscilloscope) for both positive and negative polarities using the verification module that most closely corresponds to the size package that will be tested. Refer to Annex H for example flowcharts of the procedures.

5.6.2.2 Routine verification frequency

Initially, upon tester qualification or requalification, routine waveform verification should be completed at least once per shift. If CDM stress testing is performed on consecutive shifts, waveform checks at the end of one shift may also serve as the initial check for the following shift.

Longer periods between routine waveform checks may be used if no changes in waveforms are observed for several consecutive checks. The test frequency and method chosen shall be documented. If, at any time, the waveforms no longer meet the specified limits, all ESD stress test data collected subsequent to the previous satisfactory waveform check shall be marked invalid and shall not be used for classification.

5.7 Waveform characteristics

The waveforms shall appear as shown in Figure 2 for both the positive polarity and its inverse for the negative polarity. The average waveform parameters (including I_p) as gathered by the method of 5.4 shall meet the specifications in Table 1 for a 1 GHz oscilloscope and Table 2 for a high-bandwidth oscilloscope. If a high-bandwidth oscilloscope is used for qualification, quarterly and routine waveform verifications, the 1 GHz requirements need not be considered.

Table 1 – CDM waveform characteristics for a 1 GHz bandwidth oscilloscope

1 GHz BW oscilloscope		**Test condition**									
		TC 125		TC 250		TC 500		TC 750		TC 1 000	
Verification module	Sym.	Small	Large	Small	Large	Small	Large	Small	Large	Small	Large
Peak current (A)	I_p	1,0 to 1,6	1,9 to 3,2	2,1 to 3,1	4,2 to 6,3	4,4 to 5,9	9,1 to 12,3	6,6 to 8,9	13,7 to 18,5	8,8 to 11,9	18,3 to 24,7
Rise time (ps)	t_r	< 350	< 450	< 350	< 450	< 350	< 450	< 350	< 450	< 350	< 450
Full width at half maximum (ps)	FWHM	325 to 725	500 to 1 000	325 to 725	500 to 1 000	325 to 725	500 to 1 000	325 to 725	500 to 1 000	325 to 725	500 to 1 000
Undershoot (A, max. 2nd peak)	I_{p2}	<70 % I_p	<50 % I_p	<70 % I_p	<50 % I_p	<70 % I_p	<50 % I_p	<70 % I_p	<50 % I_p	<70 % I_p	<50 % I_p

Table 2 – CDM waveform characteristics for a high-bandwidth (≥ 6 GHz) oscilloscope

≥ 6 GHz BW oscilloscope		**Test condition**									
		TC 125		TC 250		TC 500		TC 750		TC 1 000	
Verification Module	Sym.	Small	Large	Small	Large	Small	Large	Small	Large	Small	Large
Peak Current (A)	I_p	1,4 to 2,3	2,3 to 3,8	2,9 to 4,3	4,8 to 7,3	6,1 to 8,3	10,3 to13,9	9,2 to 12,4	15,5 to 20,9	12,2 to 16,5	20,6 to 27,9
Rise time (ps)	t_r	< 250	< 350	< 250	< 350	< 250	< 350	< 250	< 350	< 250	< 350
Full width at half maximum (ps)	FWHM	250 to 600	450 to 900	250 to 600	450 to 900	250 to 600	450 to 900	250 to 600	450 to 900	250 to 600	450 to 900
Undershoot (A, max. 2nd peak)	I_{p2}	<70 % I_p	<50 % I_p	<70 % I_p	<50 % I_p	<70 % I_p	<50 % I_p	<70 % I_p	<50 % I_p	<70 % I_p	<50 % I_p

NOTE The voltages of the test conditions 125 to 1 000 producing the specified peak current ranges are adjusted from previous classification test voltages of 125 V, 250 V, 500 V, 750 V and 1 000 V, respectively. Annex D describes this relationship between such voltages and ferrite-free tester set voltages. Tester adjusted field plate voltages to achieve these current ranges for the ferrite-free tester platform in this document can vary somewhat between testers. Annex H describes two voltage adjustment methods.

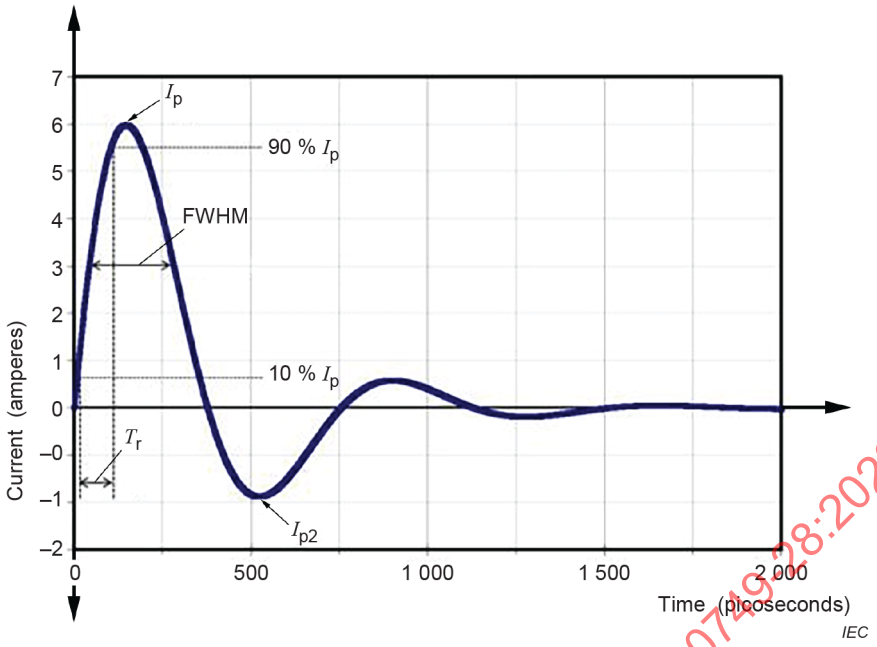


Figure 2 – CDM characteristic waveform and parameters

5.8 Documentation

Retain the waveform records for tester qualification according to internal company policy. For tester requalification, quarterly waveform verification and routine waveform verification, keep the records until the next set of waveforms are collected, or according to internal company policy.

5.9 Procedure for evaluating full CDM tester charging of a device

5.9.1 As defined in 4.1.5, the charging resistor should nominally be 100 MΩ or greater. If the resistor is too large, an added charging delay may be necessary to fully charge the device. To determine if an added delay is needed, follow the procedure in 5.9.2.

5.9.2 Using the large verification module, follow the procedure below.

a) Set the field plate voltage at +250 V (any voltage can be used as the objective is to monitor I_p).

b) With the pre- and post-charge delay both set to 0 ms, collect 10 waveforms and record the I_p from each. Calculate the average I_p of the waveforms.

c) With the pre-charge delay set to 500 ms (and post-charge delay remaining at 0 ms), collect ten waveforms, record the I_p from each. Calculate their average I_p of the waveforms.

d) Compare the average I_p value from the 0 ms charge delay and the 500 ms charge delay. If the average I_p is the same for both measurements, then a device of the same or lower capacitance as the large verification module are receiving a full charge. If the average I_p with 0 ms charge delay and 500 ms charge delay do not match, refer to the informative Annex I for a procedure to determine the appropriate default charge delay to add to the system.

e) Even if the two average I_p values above match, very large packaged devices (larger capacitance than the large verification module) may still require a delay in order to receive a full charge. Since device package technologies vary widely, there are no exact dimensions for how a particular package I_p may compare to the large verification module I_p for the evaluation described above.

f) To determine if a very large packaged device may still require a charge delay, steps a) to d) above can be repeated using the ground pin of a device. If the average I_p with 0 ms charge delay and 500 ms charge delay do not match, refer to the informative Annex I for a procedure to determine the appropriate charge delay.

In addition, where CDM testers have moving parts, care should be taken by personnel to avoid contact with these moving parts during operation.

6 CDM ESD testing requirements and procedures

6.1 ~~Device handling~~ Tester and device preparation

Devices used for CDM stressing shall not have been used for any prior stress tests.

ESD damage prevention procedures shall be used before, during, and after CDM and post parametric testing.

Devices shall be clean before testing. If needed, cleaning should be completed in compliance with company-approved procedures.

NOTE Isopropanol (isopropyl alcohol) is typically used for cleaning.

The CDM tester probe and field plate / dielectric shall be clean and dry before testing. Cleaning may be performed periodically or based on waveform acceptance using isopropanol (isopropyl alcohol) with a minimum isopropanol percentage of 70 %.

6.2 Test requirements

6.2.1 Test temperature and humidity

The test shall be carried out at room temperature. Humidity at the test head should not exceed 30 % RH. Heating or cooling the device during CDM testing is not intended.

The tester should be placed in an environment where the temperature is at room temperature.

NOTE Waveform repeatability is strongly dependent on moisture content of the air and having a low relative humidity will result in a more stable waveform.

6.2.2 Device test

6.2.2.1 Pre-stress testing

Prior to ESD stressing, complete static and dynamic testing shall be performed on all submitted devices. Parametric and functional results shall be within the limits specified in the datasheet parameters.

6.2.2.2 Failure criteria

Following ESD stressing, complete static and dynamic testing shall be performed on all stressed devices. A device is considered to have failed if parametric and functional test results are not within the limits specified in the datasheet parameters. A failure may be discounted if proven by failure analysis that it is not CDM–ESD related.

NOTE 1 A change in static leakage (e.g., pin leakage, standby current) is not an adequate criterion to determine pass/fail. It can serve as an indicator for the onset of damage.

NOTE 2 If testing is to be done at multiple temperatures, perform the test first at the lowest temperature, followed by increasing the temperature in sequence (e.g. −40 °C, +25 °C, +85 °C).

6.3 Test procedures

The test procedures are as follows.

a) Unless otherwise specified, obtain a minimum of three samples that have been verified to meet their data specifications.

b) CDM testing should begin at the lowest level in Table 3, but may begin at any level. However, if the initial voltage level is higher than the lowest level in Table 3 and the device fails at the initial voltage, testing shall be restarted with three fresh devices at the next lower level.

c) For each device, apply at least one positive and one negative discharge to each pin. Allow enough time (as specified in 5.9) between discharges for the device to reach the full test voltage level. Stresses may be partitioned by polarity, using a sample size of at least three units per polarity. Pins may also be partitioned into one or more sets of samples, provided that each pin of the device is a member of at least one set. Each set shall have a minimum of three units.

For the field-induced charging method, there are two possible procedures for charging and discharging the device: single and dual. Both procedures produce equivalent results. These procedures are described in the informative Annex G.

6.4 CDM test recording / reporting guidelines

6.4.1 CDM test recording

The CDM testing procedure for a particular product shall be recorded and stored per each company's data retention procedure. Information regarding tester waveform parameters should be available upon request; refer to Clause H.3 for more information on waveform parameter recording.

6.4.2 CDM Reporting Guidelines

Product CDM test results (including package information) shall be reported and be made available in the product reliability report.

For purposes of ensuring safe handling information for manufacturing control in an ESD protected area, it is highly recommended that publicly available product datasheets report CDM classifications.

6.5 Testing of Devices in Small Packages

Integrated circuits and discrete semiconductors (ICDS) in very small packages are very difficult to test for CDM and seldom fail CDM testing due to their small capacitance. It is not possible to specify a package dimension below which CDM testing is not needed as different technologies, design styles, and protection strategies have different susceptibilities to charged device events. In the absence of other information, all ICDS shall be tested. However, Annex C defines an optional procedure for establishing an integrated circuit capacitance C_{Small} for a specific technology and design flow. For devices with capacitance below C_{Small}, CDM testing is no longer required. ICDS with capacitance below C_{Small} and which satisfy the requirements of Annex C shall be considered to have a CDM passing level of TC 750 (Classification Level C2b in Table 3).

7 CDM classification criteria

ESD sensitive (ESDS) devices are classified according to the test procedure described in this document. CDM test results are specific to the particular package type used. The device classification is the highest ESD stress voltage level (both positive and negative polarities) at which a sample of at least three devices has passed full static and dynamic testing as per data sheet parameters following ESD testing. The CDM ESDS device classification levels are presented in Table 3.

Table 3 – CDM ESDS device classification levels

Classification level [a]	Classification test condition (in volts) [b]
C0a	< 125
C0b	125 to < 250
C1	250 to < 500
C2a	500 to < 750
C2b	750 to < 1 000
C3	≧ 1 000 [c]

[a] Use the "C" prefix to indicate a CDM classification level.

[b] The Classification Test Condition is not equivalent to the actual set voltage of the tester. See 5.6.1 and Annex H for further details.

[c] For test conditions above 1 000 V, depending on geometry of the device package, corona effects can limit the actual pre-discharge voltage and discharge current.

Annex A
(normative)

Verification module (metal disc) specifications and cleaning guidelines for verification modules and testers

A.1 Tester verification modules and field plate dielectric

The verification modules (metal discs) shall be made of brass, plated with nickel or gold/nickel, and may optionally have a gold flash coating over the nickel. They shall be manufactured to the dimensions specified in Table A.1 and shall be verified once before the initial use by either the manufacturer or user.

Caution shall be exercised during the manufacture of the discs so that they are free from burrs. If the perimeter of the disc has burrs, arcing may occur which may alter the results.

The field plate dielectric is chosen (see 4.1.4) to result in a capacitance measurement in the range specified in Table A.1.

Table A.1 – Specification for CDM tester verification modules (metal discs)

Disk	Small	Large
Diameter mm (inches)	8,89 ± 0,127 (0,350 ± 0,005)	25,4 ± 0,127 (1,000 ± 0,005)
Thickness mm (inches)	1,27 ± 0,05 (0,05 ± 0,002)	1,27 ± 0,05 (0,050 ± 0,002)
Surface flatness variation mm (inches)	≤ 0,127 (0,005)	≤ 0,127 (0,005)
Capacitance at 1 MHz (pF)	6,8 ± 5 %	55 ± 5 %

A.2 Care of verification modules

To avoid charge loss in verification modules during charged device model (CDM) evaluation, the verification modules should be cleaned using isopropanol (isopropyl alcohol, IPA) swabs for about 20 s as approved by the local safety organization, and dried in a moderate air stream to prevent charge leakage during test operation. Verification modules should be handled so as to maintain cleanliness.

The capacitance of the small and large verification modules (metal discs) shall be measured according to the procedure in Annex B, and shall conform to the values specified in Table A.1.

The tester should be cleaned periodically with isopropanol to remove any surface contamination that could result in charge loss. Particular attention should be paid to the discharge probe and field plate dielectric on which the device is placed.

Cleaning with isopropyl alcohol swabs can leave the surface moist for some period of time after the cleaning. The moisture can provide an unintended leakage path if present during the test. It is important to dry all surfaces after cleaning either by allowing sufficient time for the surfaces to dry or using forced air flow to evaporate the moisture.

Annex B
(normative)

Capacitance measurement of verification modules (metal discs) sitting on a tester field plate dielectric

a) The capacitance of the verification modules shall be measured in-situ (inside the CDM simulator), but can also be measured outside of the CDM simulator as guidance.

b) The small verification module is placed on the dielectric layer which is in direct contact with the surface of the grounded metallic field plate. Ensure there is no air space between the module and the dielectric layer, and also no air space between the dielectric layer and the metallic field plate. It is recommended that vacuum be used to ensure the verification module is held in place against the field plate dielectric.

c) Ensure the capacitance meter is "zeroed out" prior to measurement.

d) Connect the two leads from the capacitance meter (CP) as follows: One metallic lead/cable from the CP is connected to an exposed point on the field plate. The second metallic lead/cable from the CP is connected to the top of the verification module (in the centre). Measure the capacitance of the module to the grounded field plate. The capacitance value of the verification module shall be within the value specified in Table A.1.

e) Repeat steps a) to d) using the large verification module on the dielectric.

NOTE Placement of the CP meter leads can cause changes in the measured capacitance. One ~~recommended~~ preventive technique for each verification module is to take a first measurement as outlined in item d)and then take a second measurement with the verification module lead/cable just above, but not touching, the verification module. The second reading is subtracted from the first to result in the true measured value.

It is recommended to use a meter with "guarded leads".

Annex C
(normative)

Testing of small package integrated circuits and discrete semiconductors (ICDS)

C.1 Testing rationale

This annex describes a procedure for setting a capacitance limit C_{small}, below which small package integrated circuits and discrete semiconductors no longer need to be tested for CDM. ICDS in very small packages are very difficult to test, due to the challenge of handling small devices. Very small ICDS also have very low capacitance to surroundings, including during CDM testing. With a small capacitance very little charge is transferred during a CDM event, either in a factory environment or during CDM testing. Small package ICDS therefore seldom fail during CDM testing. This does not, however, mean that there is no CDM risk for small package ICDS. The charge transferred during a small package CDM event can be small but the peak currents remain high, usually over an amp since the RLC equivalent circuit of a CDM event results in a very narrow, but still high current pulse. It is very difficult to set a minimum package dimension or capacitance for CDM testing because CDM failure levels depend on a wide variety of variables, including those listed below.

– capacitance between the ICDS and the field plate
– the technology used to fabricate the device
  - advanced low voltage technologies have thin gate oxides with low breakdown voltage and can be more susceptible to CDM damage without a proper protection scheme
  - high voltage technologies have diffusions which can be subject to CDM damage
– ESD protection circuits used in the device
– general ESD protection strategy used
– design style used to design the device
– thoroughness of ESD design rule checks
– package type which can influence inductance in the CDM current path

C.2 Procedure for Determining C_{small}

The following procedure can be used to determine a limit, C_{small} at and below which CDM testing is not required for a particular integrated circuit technology:

– Choose at least 5 ICDS designs from a technology, with varying package sizes
– The requirements for circuits to be considered from the same technology are given in C.3
– Measure the capacitance between each ICDS substrate, usually the ground pin, and the CDM tester's field plate when the ICDS is in the position for CDM testing, using the procedure in Annex B for measuring the capacitance of the verification modules.

Packages shall be at least 4 times the size of the vacuum hole in the dielectric layer or the metal field plate, whichever is larger. If the package is less than 4 times the size of the vacuum hole a test fixture which holds the package against the dielectric is used. At this time, there is no universally recognized method for testing CDM capability on packages that are less than 4 times the size of the vacuum holes. Techniques including mechanical methods for holding the package made of FR4 with the package not over vacuum holes, or packaging die in a different package, have been used.

– A separate test fixture can be used for measuring the capacitance if it uses the same thickness and material for the field plate dielectric layer as the CDM tester.
– Perform CDM testing at TC 1 000 for 3 samples in accordance with 6.3c) for each of the 5 ICDS designs.
– The ICDS capacitance, at which all ICDS with that capacitance and lower all pass CDM TC 1 000, is C_{small}.

To ensure there is no air space between the integrated circuit and the dielectric layer, and also no air space between the dielectric layer and the metallic field plate, the use of vacuum is recommended.

ICDS with substrate to CDM tester field plate capacitance equal to or less than C_{small} do not need to be tested for CDM if the following conditions are met:

– The ICDS has passed HBM according to requirements of the technology. This indicates the expected protection circuit is present.
– The ICDS uses the same technology, as defined in C.3, as used to determine C_{small}.
– ICDS devices not tested because their capacitance is below C_{small} and satisfy the above requirement shall be considered to have a CDM passing level of TC 750 (Classification Level C3b).

C.3 ICDS Technology requirements

ICDS are considered to be from the same technology if the following conditions are met:

- the ICDS shall use the same wafer fabrication flow.
- all ICDS shall use the same ESD protection circuits and ESD design rules.
- all ICDS shall have their substrate to CDM tester field plate capacitance measured using the procedures in Annex B.
- a separate test fixture which simulates the CDM tester field plate and dielectric can be used.
- calculated substrate to field plate capacitance can be used if the calculation procedure has been verified with measurements using the procedures in Annex B.

Annex D
(informative)

CDM test hardware and metrology improvements

The goal of this document is to reduce duplication of effort and confusion by developing a single agreed standard, correcting deficiencies in previous CDM standards whilst maintaining similar stress levels as those previous standards. This required significant hardware and metrology changes to arrive at an improved joint standard. This informative annex describes the motivations for these updates.

The major changes in this test method are listed below.

- Some details of the required waveforms have been modified to better match the high-frequency behaviour of CDM events.
- The test method now requires that the test head not include ferrites or other circuits to modify the high-frequency behaviour of the CDM pulse.
- The test method now requires that tester qualification and requalification be performed with a 6 GHz or faster oscilloscope, and recommends the use of 6 GHz or faster oscilloscopes for quarterly and regular tester verification if a fast oscilloscope is available.
- The tester qualification and verification procedures have been modified to give more flexibility in the field plate voltage settings to arrive at the required peak currents.
- The specification of test levels by voltage has been replaced by a series of test conditions which are related to the previous voltage levels.

When the original CDM test method was developed in the late 1980s, single-shot oscilloscopes with 1 GHz and higher bandwidths were expensive, not readily available and less capable than those available today. The result was that the original waveforms used to develop previous standards had a wider half-width than was characteristic of the actual CDM event. As measurement capability improved and the high frequency behaviour of test heads was improved, tester manufacturers found the peak width at half-height was narrower than allowed previously. In order to meet the peak width at half-height, ferrite beads were often added to the test head to bring the current waveforms into compliance. When oscilloscopes in the 4 GHz to 8 GHz range become readily available, it was found that the ferrite beads, which simply broadened the peak width when measured with a 1 GHz oscilloscope, created undesirable high-frequency harmonics with undesirable consequences. A primary goal in the development of this document was to remove the ferrite beads from the CDM test heads and to modify the waveform requirements to allow this change.

The 1 GHz oscilloscope specified previously is only marginally fast enough to capture CDM events and significantly reduces the measured peak current of the captured waveforms, especially for the small verification module and small integrated circuits. Accurate peak current measurements require the use of a measurement chain with 6 GHz or higher bandwidth, and the new joint standard reflects this requirement for CDM tester qualification. A 1 GHz oscilloscope was considered adequate for routine waveform verification, and that option is still available in the new standard, although the higher bandwidth oscilloscope is recommended if it is available.

The increased flexibility between the required peak current values and the field plate voltage to produce the peak current has been implemented for two reasons: to better match current practice, and to achieve similar stress levels as the legacy standards.

Previous standards specified the CDM tester geometry, as well as the required waveforms at specified field plate voltages. CDM tester manufacturers quickly found that it was often impossible to obtain the required peak current values with the required geometry and the specified field plate voltage. The manufacturers introduced adjustments to the field plate voltage so that the required waveforms were obtained when the specified voltage was selected in the CDM tester software. This adjustment was reasonable since it is known that it is peak current, not field plate voltage, which damages integrated circuits. The result was that when an integrated circuit passed 500 V, the field plate voltage was often considerably different than 500 V, but the intended current pulse was in fact applied to the device under test.

The removal of the ferrite beads, and the extra impedance which the beads produced, has resulted in higher peak currents than were present in legacy test methods for the same field plate voltage and tester geometry. This creates a second reason to give more flexibility in the setting of the field plate voltage to obtain the required peak currents. Since CDM failure is a result of the peak current during the CDM event, it is therefore more important that different CDM testers create the same peak current for specified test conditions rather than that the field plate voltages are the same. For this reason, the test voltages specified in the earlier standard CDM documents have been replaced by a series of test conditions producing peak currents similar to those at the specified voltages in recent previous standards.

Annex E
(informative)

CDM tester electrical schematic

Figure E.1 represents an electrical model of a CDM tester setup. CDUT is the capacitance between the DUT and the field plate, CDG is the capacitance between the DUT and the ground plane, and CFG is the capacitance between the field plate and the ground plane. The 1 Ω resistance between the pogo pin and the ground plane may be the parallel combination of the resistive probe and the coaxial cable/oscilloscope impedance as described above. The resistance of the spark which forms between the pogo pin and the DUT is assumed to be a variable resistance. The inductance of the pogo pin and spark are lumped together as a single inductor.

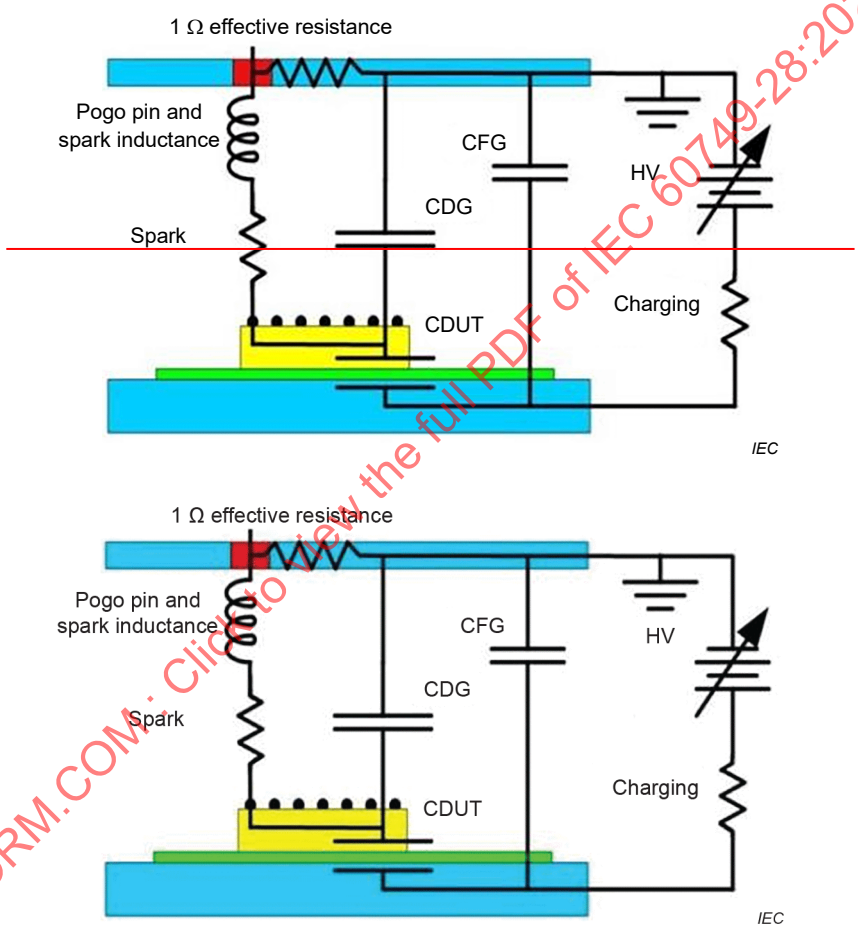


Figure E.1 – Simplified CDM tester electrical schematic

Annex F
(informative)

Sample oscilloscope setup and waveform

F.1 General

The following setup examples are based on measurements of a TC 500 waveform using a 1 GHz and 8 GHz oscilloscope. Other oscilloscopes will have different settings, but this annex should provide basic guidelines that can be used on most oscilloscopes.

F.2 Settings for the 1 GHz bandwidth oscilloscope

Vertical	200 mV/division (small verification module) or 200 mV/division (large verification module)
Timebase	400 ps/division
Trigger	300 mV small verification module or 400 mV large verification module
Impedance	50 Ω

These settings are for an oscilloscope for which the attenuation correction could not be made.

F.3 Settings for the high-bandwidth oscilloscope

Vertical	2 V/division (small verification module) or 2 V/division (large verification module)
Timebase	400 ps/division
Trigger	3 V small verification module or 4 V large verification module
Impedance	50 Ω

These settings are for an oscilloscope for which the attenuation correction was made in the oscilloscope software.

F.4 Setup

Attach the 20 dB attenuator to the oscilloscope. Attach the cable to the end of the attenuator and to the voltage output of the CDM tester.

NOTE The 20 dB attenuator is a 10× attenuator. If the oscilloscope does not automatically compensate for this, the measurements need to be multiplied by 10 to get the correct reading (e.g. from the small ~~coin below~~ verification module used in figure F.1, 532 mV = 5,32 A peak current).

F.5 Sample waveforms from a 1 GHz oscilloscope

Sample waveforms from a 1 GHz oscilloscope are illustrated in Figure F.1 and Figure F.2.

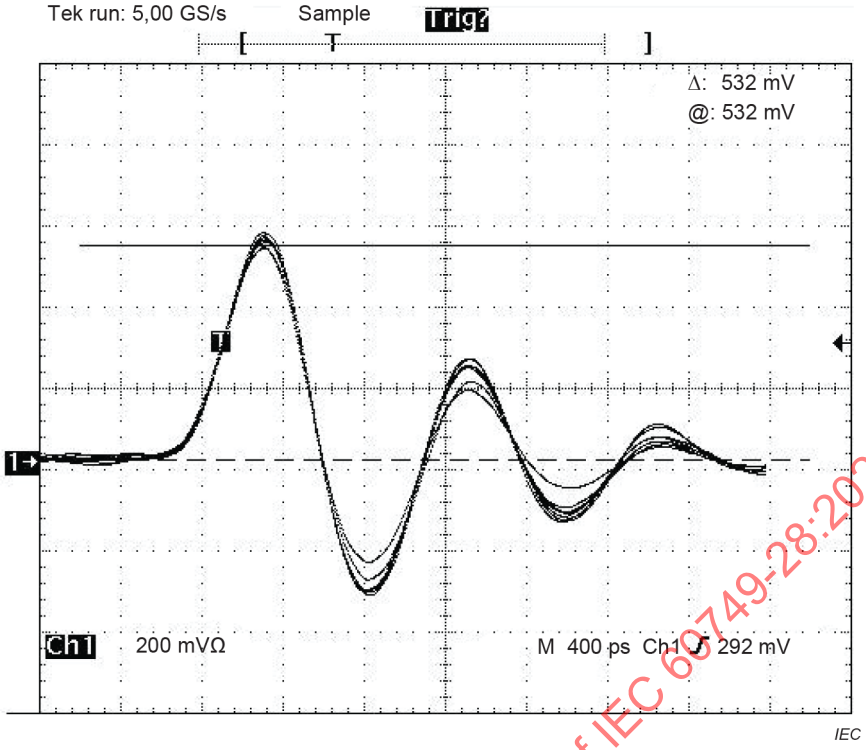


Figure F.1 – 1 GHz TC 500, small verification module

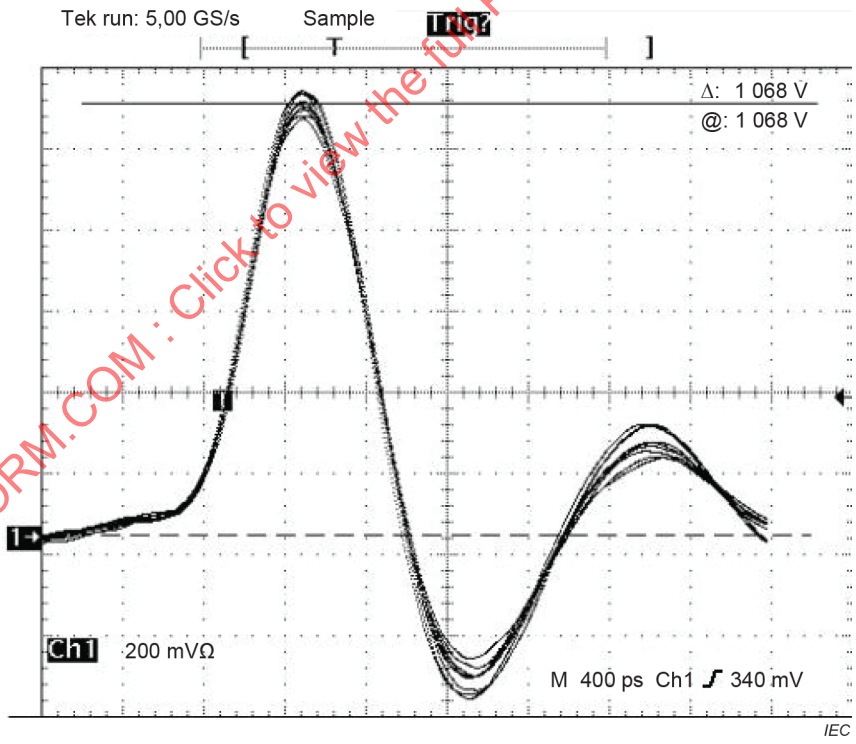


Figure F.2 – 1 GHz TC 500, large verification module

F.6 Sample waveforms from an 8 GHz oscilloscope

Sample waveforms from an 8 GHz oscilloscope are illustrated in Figure F.3 and Figure F.4.

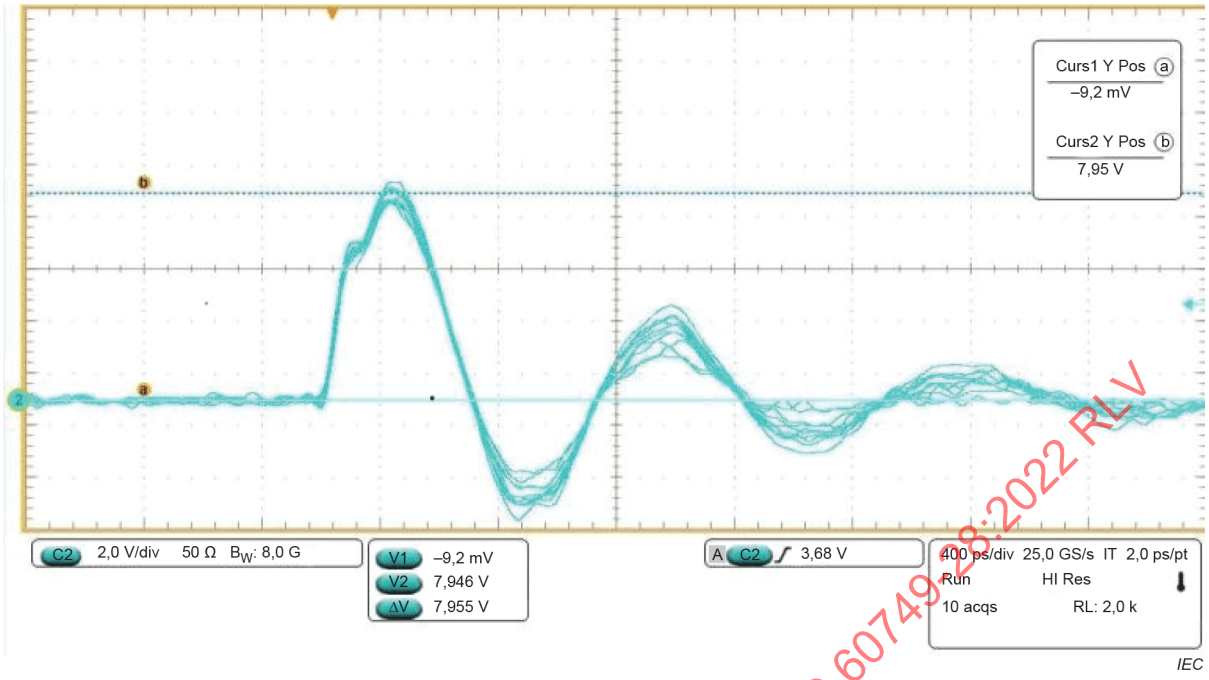


Figure F.3 – 8 GHz TC 500, small verification module (oscilloscope adjusts for attenuation)

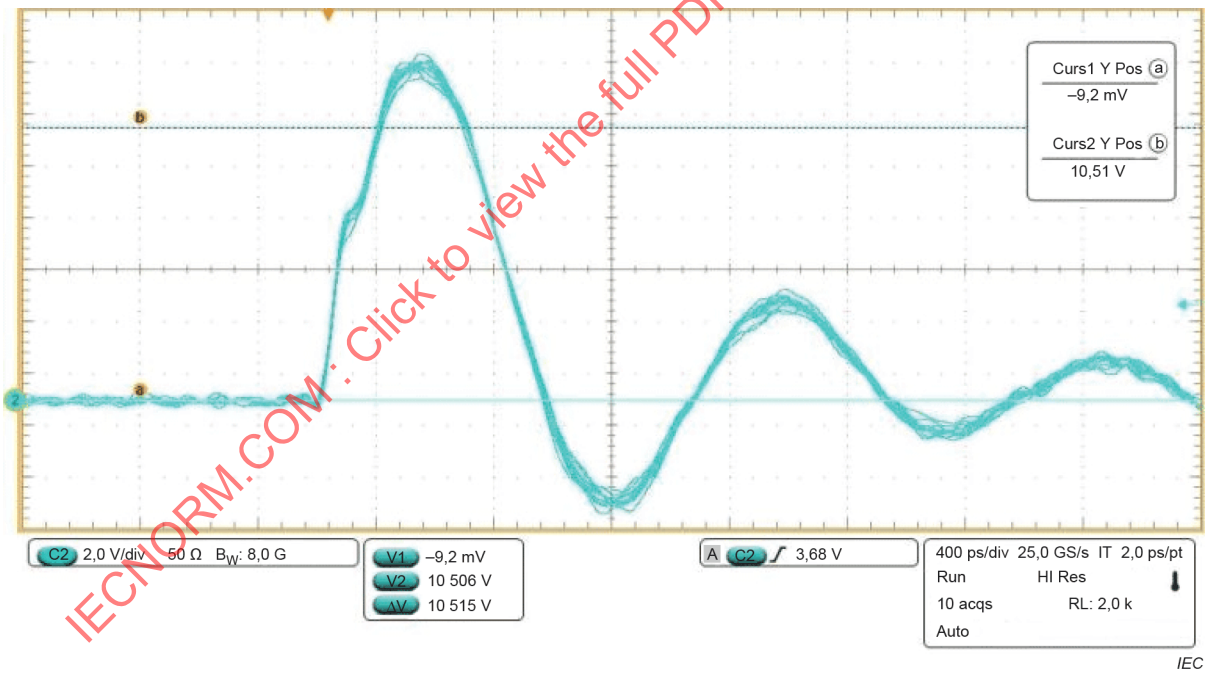


Figure F.4 – GHz TC 500, large verification module (oscilloscope adjusts for attenuation)

Annex G
(informative)

Field-induced CDM tester discharge procedures

G.1 General

Annex G describes the two types of discharge procedures used in field-induced CDM test equipment.

G.2 Single discharge procedure

The single positive and single negative discharges can be applied with two individual discharges using this sequence of steps producing the sequence of charging/discharging events as illustrated in Figure G.1.

a) Place the uncharged DUT on the field plate and align it.

b) The field voltage is established by raising the voltage on the field plate to the specified stress level.

c) The first discharge is made by lowering the pogo pin to the DUT (see Figure G.1).

d) The pogo pin continues to descend until it makes physical contact with the device pin under test (PUT) to ensure full charge transfer and to provide a conduction path to ground.

e) Then the voltage on the field plate is slowly (resistively) returned to zero, which completely removes the charge that was transferred to the DUT during the first CDM discharge.

f) The pogo pin is returned to its starting (separated) position (see Figure G.1) before the voltage of the same or opposite polarity is applied to the field plate for subsequent discharges.

g) Repeat for each pin to be tested.

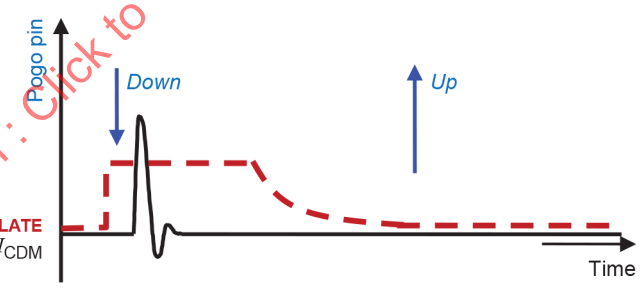


Figure G.1 – Single discharge procedure (field charging, I_{CDM} Pulse, and slow discharge)

G.3 Dual discharge procedure

The single positive and single negative discharges can be applied with one pair of alternating polarity discharges using this sequence of steps producing the sequence of charging/discharging events as illustrated in Figure G.2.

a) Place the uncharged DUT on the field plate and align it.

b) The field voltage for the positive stress is established by raising the voltage on the field plate to the specified stress level.

c) The first discharge is made by lowering the pogo pin to the DUT (see Figure G.2).

d) The pogo pin continues to descend until it makes physical contact with the DUT. This is to ensure full charge transfer and to provide a conduction path to ground.

e) The pogo pin is returned to its starting separated position (see Figure G.2), leaving the device with a net charge.

f) The voltage on the field plate is slowly (resistively) returned to zero, which completely removes the charge on the field plate. The DUT will still have a net charge.

g) The pogo pin is lowered (the second down arrow to the right in Figure G.2) a second time for the second discharge, which will be of opposite polarity and the same magnitude.

h) Repeat for each pin to be tested.

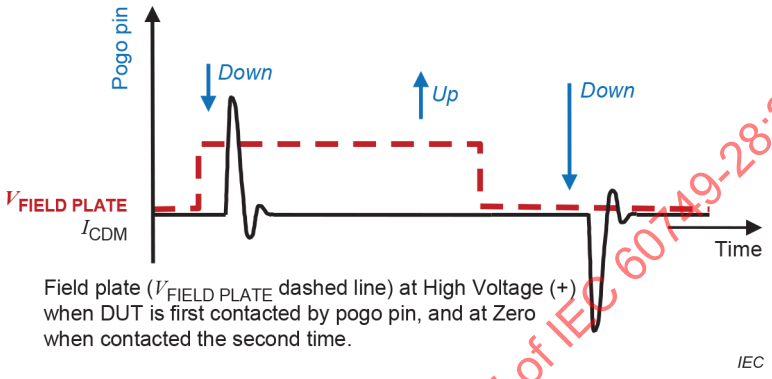


Figure G.2 – Dual discharge procedure (field charging, 1st I_{CDM} pulse, no field, 2nd I_{CDM} pulse)

Annex H
(informative)

Waveform verification procedures

H.1 Factor/offset adjustment method

This procedure aligns the tester for direct software voltage input of the test condition for the full alignment range. This method may not allow for alignment of each test condition with the target mid-range of I_p as shown in Table 1 or Table 2, but it is the easiest to use in a lab environment with multiple testers, as the software voltage entered matches the test condition target level and does not require linear interpolation/extrapolation for test conditions other than the five levels listed in Table 1 or Table 2.

The requirements/details of this method are as follows:

– a single factor/offset is used across the entire test condition range;
– a different factor/offset can be used for each polarity;
– the same factor/offset shall be used for both large and small verification modules.

Figure H.1 below depicts the waveform verification flow for qualification/re-qualification and quarterly checks, while Figure H.2 shows the flow for routine verifications. Table H.1 shows an example of the data that should be recorded.

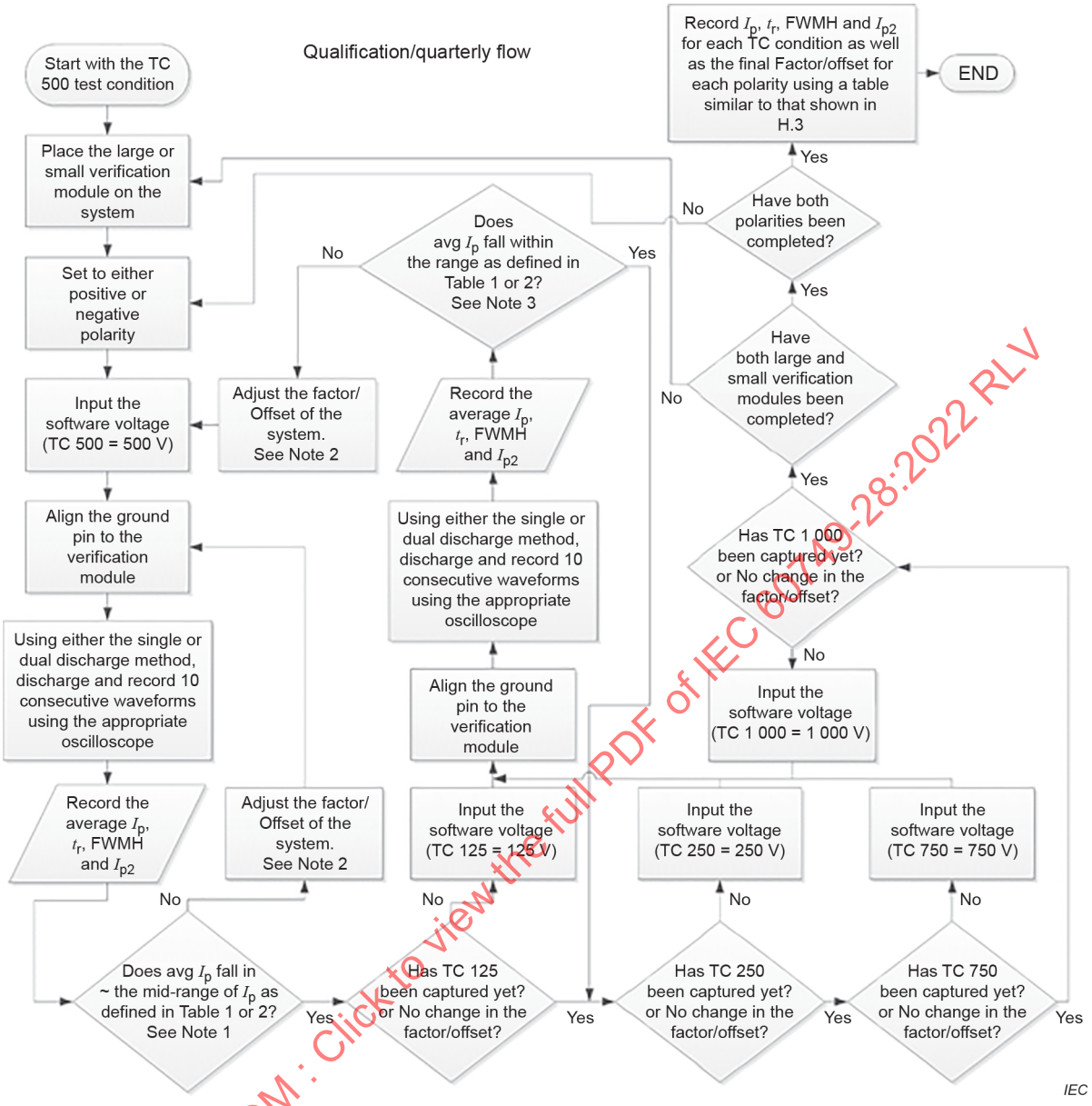


Figure H.1 – An example of a waveform verification flow for qualification and quarterly checks using the factor/offset adjustment method

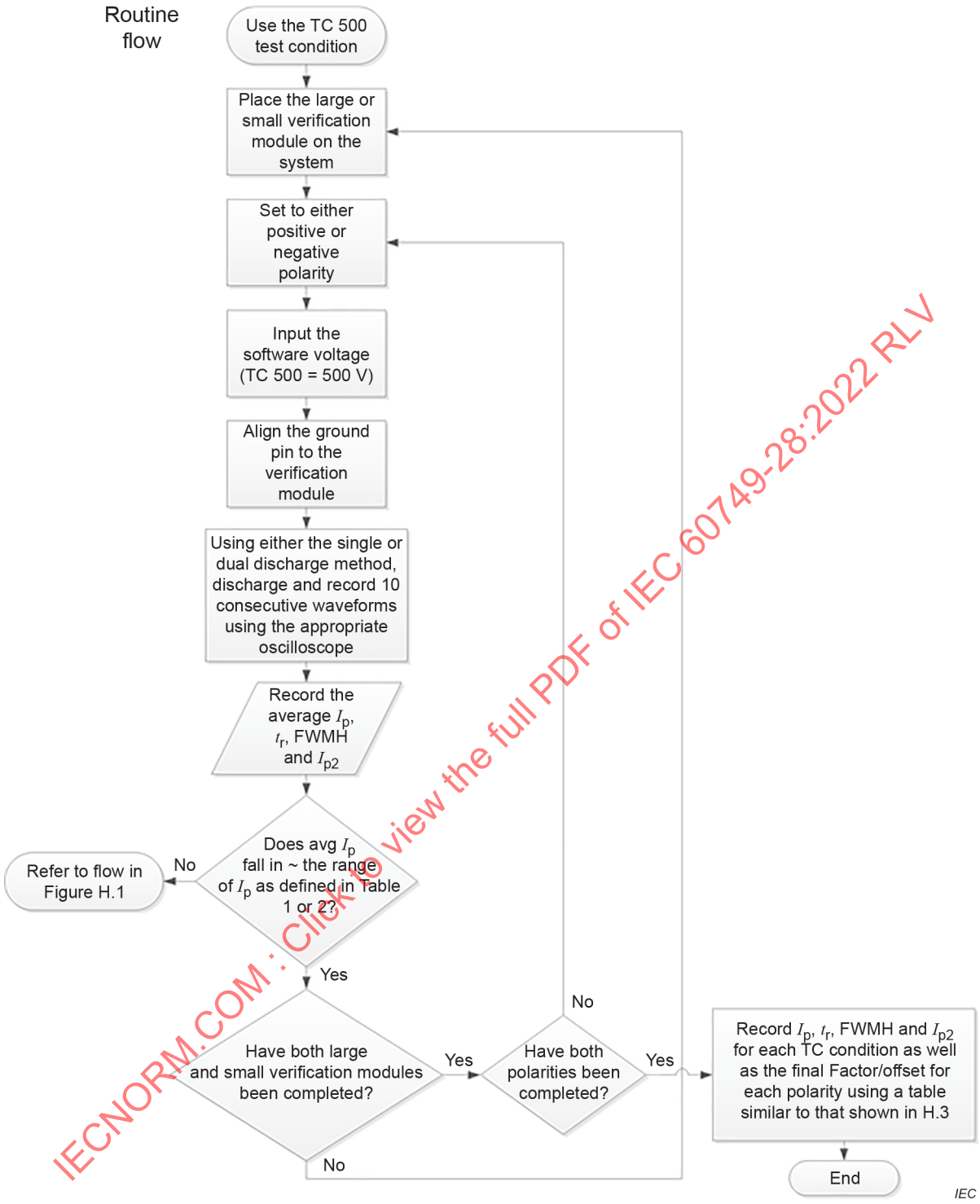


Figure H.2 – An example of a waveform verification flow for the routine checks using the factor/offset adjustment method

NOTE 1 Targeting to the mid-range of TC 500 is a starting point for adjustment of the field plate voltage. Based on the results of the other test conditions (TC 125/250/750/1 000) the I_{peak} can end up higher or lower than the mid-range value on TC 500. As shown in Figure H.3, adjustments in the factor/offset can shift the I_{peak} higher or lower.

NOTE 2 To properly calibrate systems, tester manufacturers have implemented a secondary "adjustment" parameter as an offset from the software voltage setting, either represented as a voltage "multiplier" value or a percentage "offset" value which modifies the field plate voltage. The tester manufacturer can be consulted for more detail.

After several iterations through this loop, if the user finds they cannot meet the I_{peak} range as defined in Table 1 or Table 2 or the factor/offset is outside the typical documented range, the verification modules and ground pin can be cleaned and all connections checked for tightness. If this still does not work, the system vacuum can be checked or the ground pin replaced. The tester manufacturer can be contacted for more information.

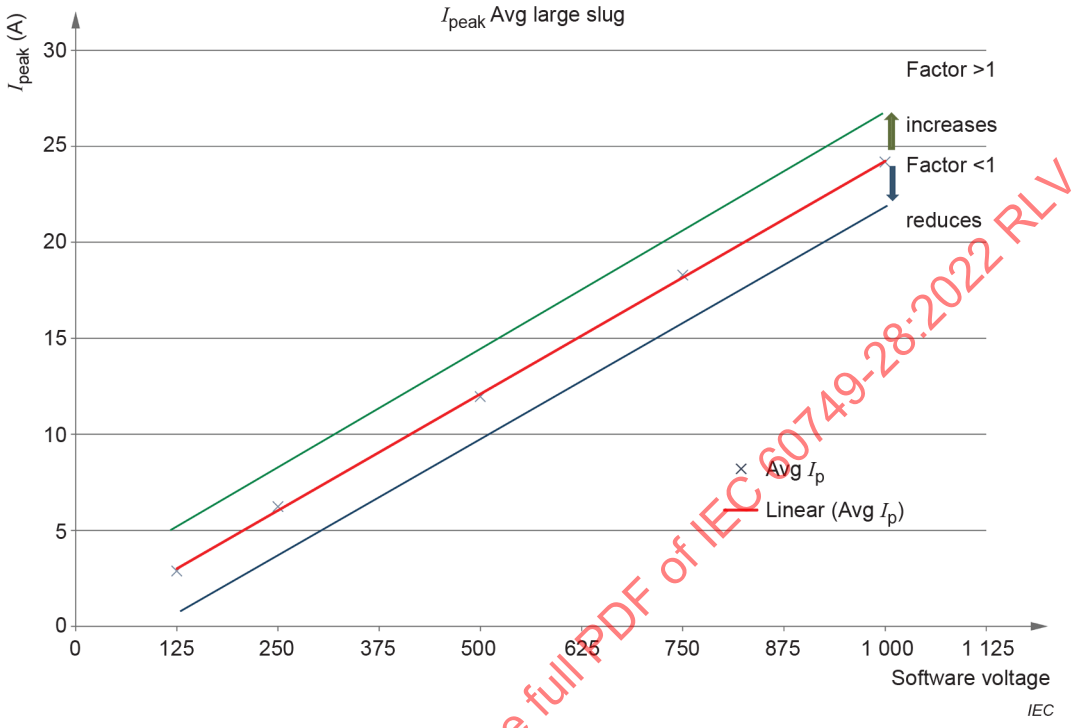


Figure H.3 – Example of average I_{peak} for the large verification module – high bandwidth oscilloscope

H.2 Software voltage adjustment method

This procedure does not adjust the factor/offset but leaves the factor/offset with a value that will not impact the field plate voltage and uses the software voltage entry as the primary adjustment of the field plate voltage. This method will allow for a much more accurate targeting of the midpoint of the I_p range as defined in Table 1 or Table 2, but creates complexity in determining the correct software voltage entry between the five test conditions. Determining software voltage entries, other than the five test condition levels, (which will be determined in this procedure) will require linear interpolation/extrapolation.

The requirements/details of this method are as follows:

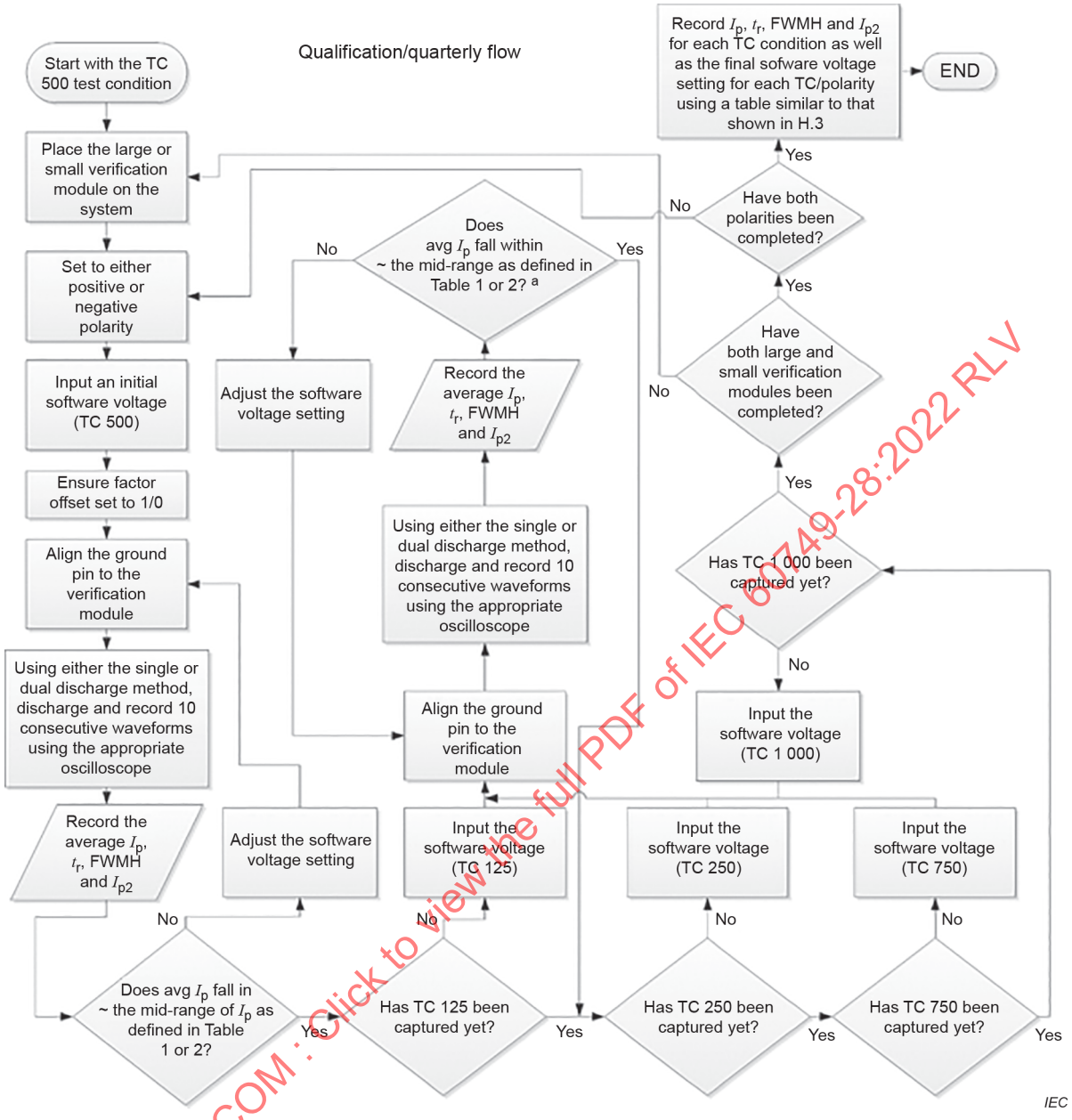
– a unique software voltage setting is determined for each test condition;

– unique voltage settings may be used for each polarity (at each test condition);

– the same software voltage setting shall be used for both large and small verification modules at each test condition;

– testing at levels other than the five test conditions will require a linear interpolation/extrapolation to determine the correct software voltage entry.

Figure H.4 below depicts the waveform verification flow for qualification/re-qualification and quarterly checks while Figure H.5 shows the flow for routine verifications. Table H.2 shows an example of the data which should be recorded.



[a] After several iterations through this loop, if the user finds they cannot meet the I_{peak} range as defined in Table 1 or Table 2 or that the software voltage setting is well outside the typical documented range, re-clean the verification modules and ground pin and check that all connections are tight. If this still does not work, check the system vacuum or look at replacement of the ground pin. Consult the tester manufacturer for more information.

Figure H.4 – An example of a waveform verification flow for qualification and quarterly checks using the software voltage adjustment method

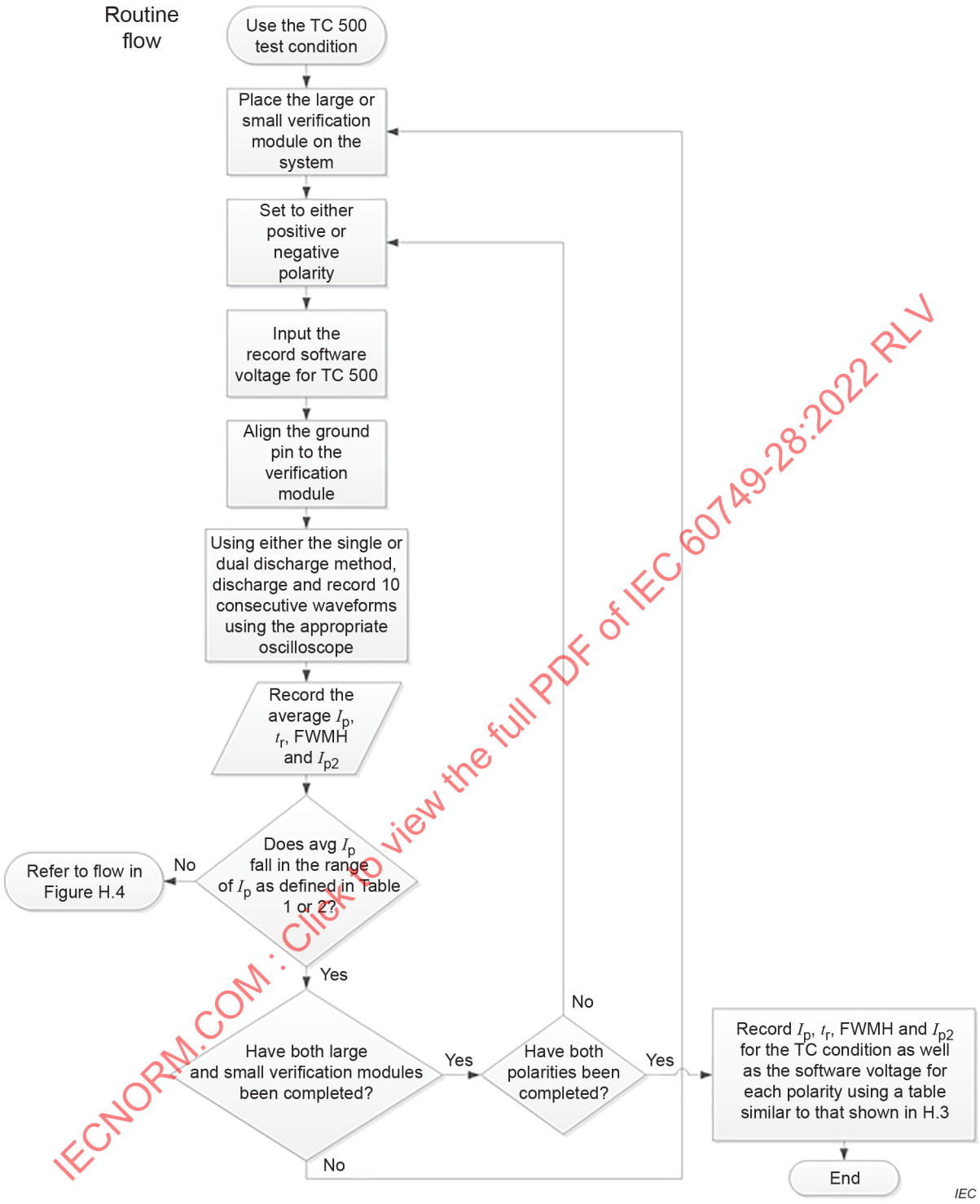


Figure H.5 – An example of a waveform verification flow for the routine checks using the software voltage adjustment method

H.3 Example parameter recording tables

Table H.1 gives an example table of CDM qualification/quarterly verification waveform parameters to be recorded for the factor/offset adjustment method.

Table H.1 – Example waveform parameter recording table for the factor/offset adjustment method

Tester – System # 1									
Polarity = positive		Scope bandwidth = 8 GHz				Factor/offset final setting = 0,82			
Module size	Date	% RH	Test cond	Software voltage	$I_{P\ AVG}$ (A)	$t_{R\ AVG}$ (ps)	T_{D}FWHM $_{AVG}$ (ps)	$I_{P2\ AVG}$ (A)	I_{P2} (% I_{P1})
Large	dd/m/yy	*X* %	TC 500	500	12,1	275	610	4,3	36 %
Small	dd/m/yy	*X* %	TC 500	500	7,30	185	400	3,7	51 %
Large	dd/m/yy	*X* %	TC 125	125	2,90	283	611	1,1	38 %
Small	dd/m/yy	*X* %	TC 125	125	1,90	201	395	1,1	58 %
Large	dd/m/yy	*X* %	TC 250	250	6,00	276	609	2,2	37 %
Small	dd/m/yy	*X* %	TC 250	250	3,70	186	397	2,1	57 %
Large	dd/m/yy	*X* %	TC 750	750	18,30	274	611	7,2	39 %
Small	dd/m/yy	*X* %	TC 750	750	11,00	190	398	6,1	55 %
Large	dd/m/yy	*X* %	TC 1 000	1 000	24,40	276	612	9,2	38 %
Small	dd/m/yy	*X* %	TC 1 000	1 000	14,60	187	399	7,4	51 %

~~Below is an example table of CDM qualification / quarterly verification waveform parameters~~

Table H.2 gives an example of CDM qualification / quarterly verification waveform parameters to be recorded for the software voltage adjustment method.

Table H.2 – Example waveform parameter recording table for the software voltage adjustment method

Tester – System # 2									
Polarity = positive		Scope bandwidth = 8 GHz				Factor/offset final setting = 1/0			
Module size	Date	% RH	Test cond	Software voltage	$I_{P\ AVG}$ (A)	$t_{R\ AVG}$ (ps)	T_{D}FWHM $_{AVG}$ (ps)	$I_{P2\ AVG}$ (A)	I_{P2} (% I_{P1})
Large	dd/m/yy	*X* %	TC 500	410	12,1	275	610	4,3	36 %
Small	dd/m/yy	*X* %	TC 500	410	7,30	185	400	3,7	51 %
Large	dd/m/yy	*X* %	TC 125	105	2,90	283	611	1,1	38 %
Small	dd/m/yy	*X* %	TC 125	105	1,90	201	395	1,1	58 %
Large	dd/m/yy	*X* %	TC 250	205	6,00	276	609	2,2	37 %
Small	dd/m/yy	*X* %	TC 250	205	3,70	186	397	2,1	57 %
Large	dd/m/yy	*X* %	TC 750	620	18,30	274	611	7,2	39 %
Small	dd/m/yy	*X* %	TC 750	620	11,00	190	398	6,1	55 %
Large	dd/m/yy	*X* %	TC 1 000	840	24,40	276	612	9,2	38 %
Small	dd/m/yy	*X* %	TC 1 000	840	14,60	187	399	7,4	51 %

Annex I
(informative)

Determining the appropriate charge delay for full charging of a large module or device

I.1 General

Annex I describes the procedure for characterizing the charge delay on the CDM tester and determining the appropriate delay (for full charging) as either the default delay for the system (if the initial large verification module checkout fails as described in 5.9) or the delay required for a very large package device.

I.2 Procedure for charge delay determination

Follow the procedure below to determine an appropriate charge delay.

Using the large verification module or the ground pin of a very large package device:

a) Set the field plate voltage at +250 V (any voltage can be used as the objective is to monitor I_p).

b) With the pre-/post-charge delay set to 0 ms, collect 10 waveforms and record the I_p from each. Calculate the average I_p of the waveforms.

c) Increase the pre-charge delay by 50 ms, collect 10 waveforms, record the I_p from each, and calculate their average I_p.

d) Continue incrementing the delay by 50 ms (a larger or smaller step can be chosen) and record the average I_p until a minimum of 500 ms charge delay.

e) Plot the results as shown in Figure I.1.

f) The appropriate charge delay results in a "saturation point" for I_p. As shown in Figure I.1, I_p for this example saturates at ~300 ms. Adding some guard band to this example would ensure that a pre-charge delay of 400 ms would be sufficient as either the default charge delay on the system (if the large verification module had been used) or as the required charge delay on a specific large package device if a large device had been used as the vehicle for the data collection.

g) For most large devices, it is expected that 500 ms will be sufficient to reach a saturation point. However, if after 500 ms, a saturation point has not been reached, repeat steps d) and e) until this occurs.

h) It is important to note that longer delay times do not "overcharge" the device but would only increase test time.

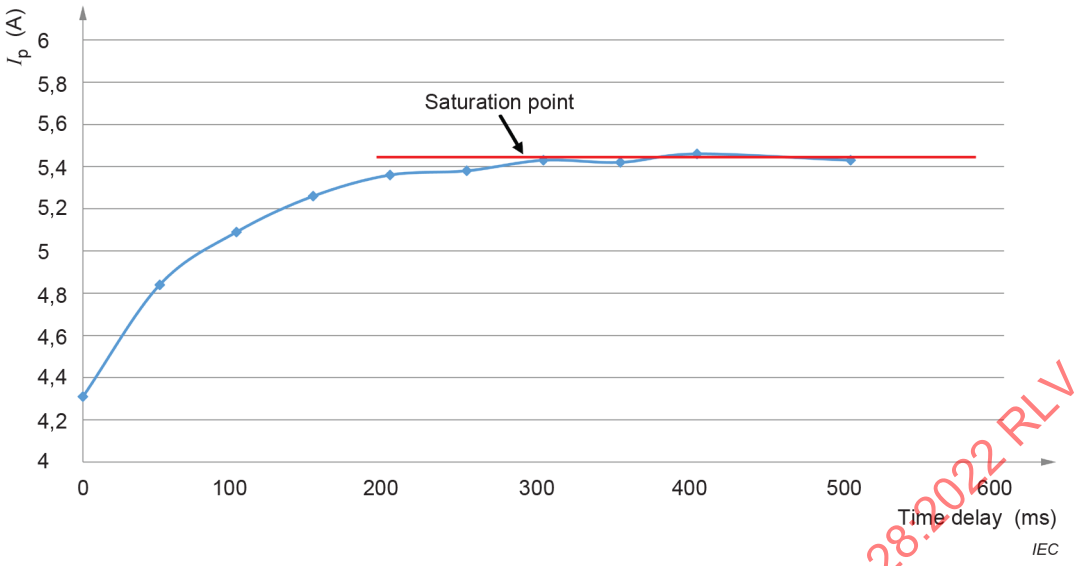


Figure I.1 – An example characterization of charge delay vs. I_p

Annex J
(informative)

Electrostatic discharge (ESD) sensitivity testing direct contact charged device model (DC-CDM)

NOTE The method identified in Annex J has not been shown to give results that correlate with results using the hardware and field-induced method specified in the body of this document.

J.1 General

Annex J describes the direct contact charged device model (DC-CDM) for the electrostatic discharge test method, which is used to evaluate the sensitivity of integrated circuits to electrostatic discharges. It is an alternative to the field-induced (FI) model.

This test method is used to reproduce and evaluate the effect of the discharge of a device.

This test method is for use on packaged devices. Where it is necessary to evaluate components that are shipped as wafers or bare chips, the components are assembled into a package similar to that expected in the final application.

This test method is classified as destructive.

J.2 Standard test module

Two types of the metal disks (listed in Table J.1), one small and one large, are used as the standard test modules, and are made of brass plated with nickel or gold/nickel and may optionally have a gold flash coating over the nickel.

The standard test modules for the field-induced CDM simulator can be cleaned in an ultrasonic bath using isopropanol for about 20 s and dried in a moderate air stream to prevent charge leakage during test operation.

Table J.1 – Dimensions of the standard test modules

Type of modules	Diameter (mm)	Thickness (mm)
Small	9,0 ± 0,1	1,3 ± 0,1
Large	25,5 ± 0,2	1,3 ± 0,1

J.3 Test equipment (CDM simulator)

J.3.1 Test equipment design

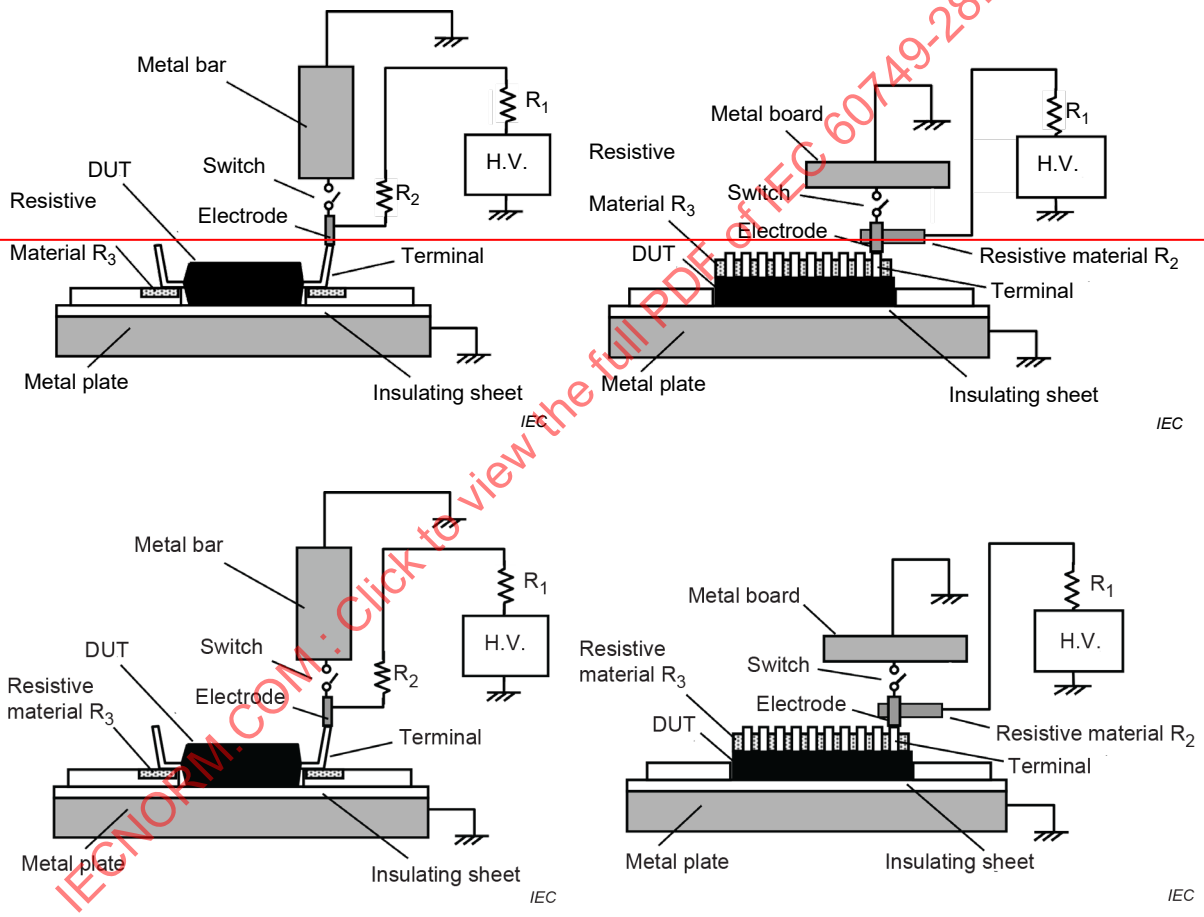
The test equipment should be designed on the basis of the test circuits described below and should satisfy the verification conditions specified in Clause J.4.

J.3.2 DUT (device under test) support

The DUT should be capable of being placed on an insulating sheet attached to a metal plate as shown in Figure J.1. The metal plate should be of sufficiently wide area to contain the DUT and should be able to maintain ground potential. The insulating sheet is 0,4 mm ± 0,04 mm in thickness, relative permittivity 4,0 ± 0,5 at 1 GHz, volume resistivity 1×10^{15} Ωm or more and with a breakdown voltage higher than the test voltage. A glass epoxy material (e.g. FR-4) is in the range of a relative permittivity of 4,0 ± 0,5 at 1 GHz.

J.3.3 Metal bar/board

The metal bar/board is connected to ground potential. The shape of the metal bar/board is a column, a square pillar, a disc or a square board. The metal bar/board is connected to the ground with a wire (connect the wire to the grounding connection on the housing of the test equipment). The test equipment should meet the verification specified in Clause J.4 by changing the size and configuration of the metal bar/board, and the length of the electrode.



a) Example of use of a metal bar

b) Example of use of a metal board and a resistive material R_2

Figure J.1 – Examples of discharge circuit where the discharge is caused by closing the switch

J.3.4 Equipment setup

All of the terminals of the DUT should be capable of maintaining the test potential of the high voltage power supply (H.V.) as shown in Figure J.1. When a high-voltage power supply is to be connected to the terminals of the DUT via a wire, a charging resistor R_1 that is capable of withstanding the test voltage is connected in series between the power supply and the terminals. Resistor R_1 should have a resistance in the range of 10 MΩ to 100 MΩ, but it can be greater

provided it meets the conditions prescribed in J.4. When a high-voltage power supply is connected to the terminals of the DUT via an electrode, a resistor/resistive material R_2 with a resistance in the range of 1 MΩ to 10 MΩ is connected in series near the electrode.

The position of R_2 is to be close to the electrode to prevent the wiring being affected during discharges. When R_2 is a resistive material, as shown in Figure J.1 b), connect with the electrode directly.

It is recommended that a resistive material R_3 should be connected to all the terminals of the DUT to ensure that the potentials of all the terminals coincide with the test voltage (see J.5.2 b)). The volume resistivity of the resistive material R_3 should be 1×10^4 Ωm to 1×10^8 Ωm. When the resistive material R_3 cannot make contact with all terminals of the DUT, as a minimum, the test terminal and power pins of the DUT should be capable of being charged (see J.4.3).

J.4 Verification of test equipment

J.4.1 General description of verification test equipment

The verification test measures the discharge current flow to the metal bar/board from the standard test module as shown in Figure J.2.

In practice, for the actual verification, a current sensor, such as the current probe, is added to the equipment. The idealised parameters, without current sensor, are specified in Figure J.3, Table J.2 and Table J.3.

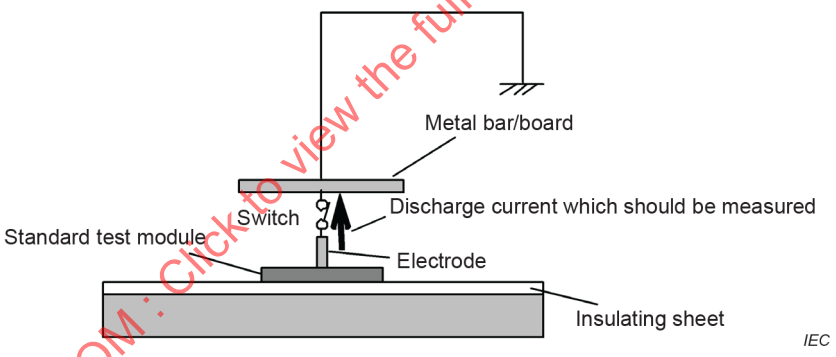


Figure J.2 – Verification test equipment for measuring the discharge current flowing to the metal bar/board from the standard test module

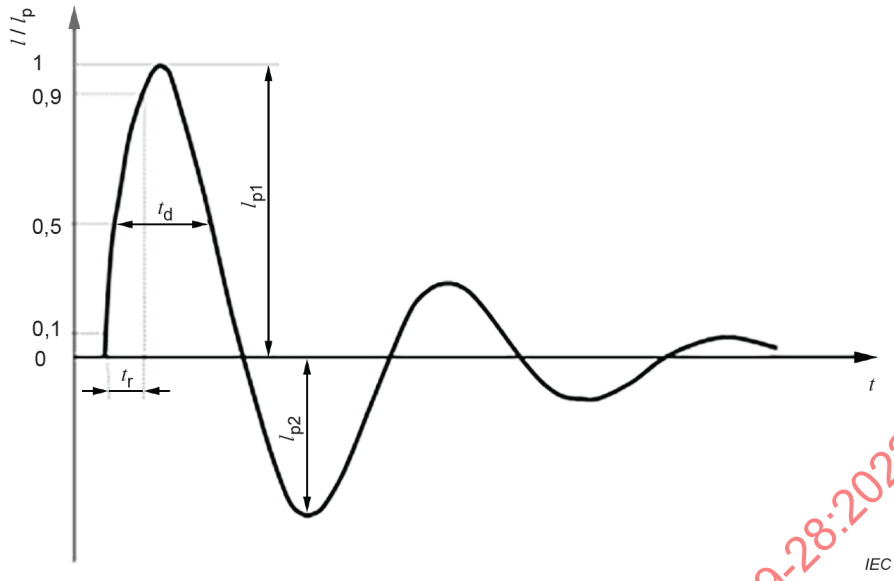


Figure J.3 – Current waveform

Table J.2 – Specified current waveform

Parameter	Unit	Symbol	Specified values	
			Small standard test module	Large standard test module
Rise time	ps	t_r	≤ 350	≤ 450
Pulse width	ps	t_d	325 to 725	500 to 1 000
Peak current	A	I_{p1}	(see Table J.3)	(see Table J.3)
Undershoot current	A	I_{p2}	< 0,7 × I_{p1}	< 0,5 × I_{p1}

Table J.3 – Range of peak current I_{p1} for test equipment

Verification voltage (V)	Values of peak current I_{p1} (A)	
	Small standard test module	Large standard test module
125	1,1 to 1,6	2,1 to 3,1
250	2,2 to 3,1	4,2 to 6,2
500	4,4 to 6,2	8,4 to 12,4
750	6,6 to 9,3	12,6 to 18,6
1 000	8,8 to 12,4	16,8 to 24,8

J.4.2 Instruments for measurement

An oscilloscope with a single shot bandwidth of at least 1 GHz (2 GHz is recommended) with 50 Ω input impedance is used. When a sampling-type oscilloscope is used, a minimum real-time sample rate of 5 GHz is used.

A current probe with bandwidth of at least 2 GHz is used to evaluate the current measurement circuit described in J.4.3, prior to verification of the test equipment.

J.4.3 Verification of test equipment, using a current probe

J.4.3.1 Verification circuit

In order to measure the applied voltage using a current probe, a metal wire of 8 mm in length is added to the standard test module specified in J.2. As shown in Figure J.4, the test equipment is verified by measuring the discharge current from a standard test module to the metal bar/board with the oscilloscope and current probe specified in J.4.2. Since the current probe will not be able to withstand the high voltage required by this method, it will be necessary to maintain the insulation between the current probe and the high-voltage circuit.

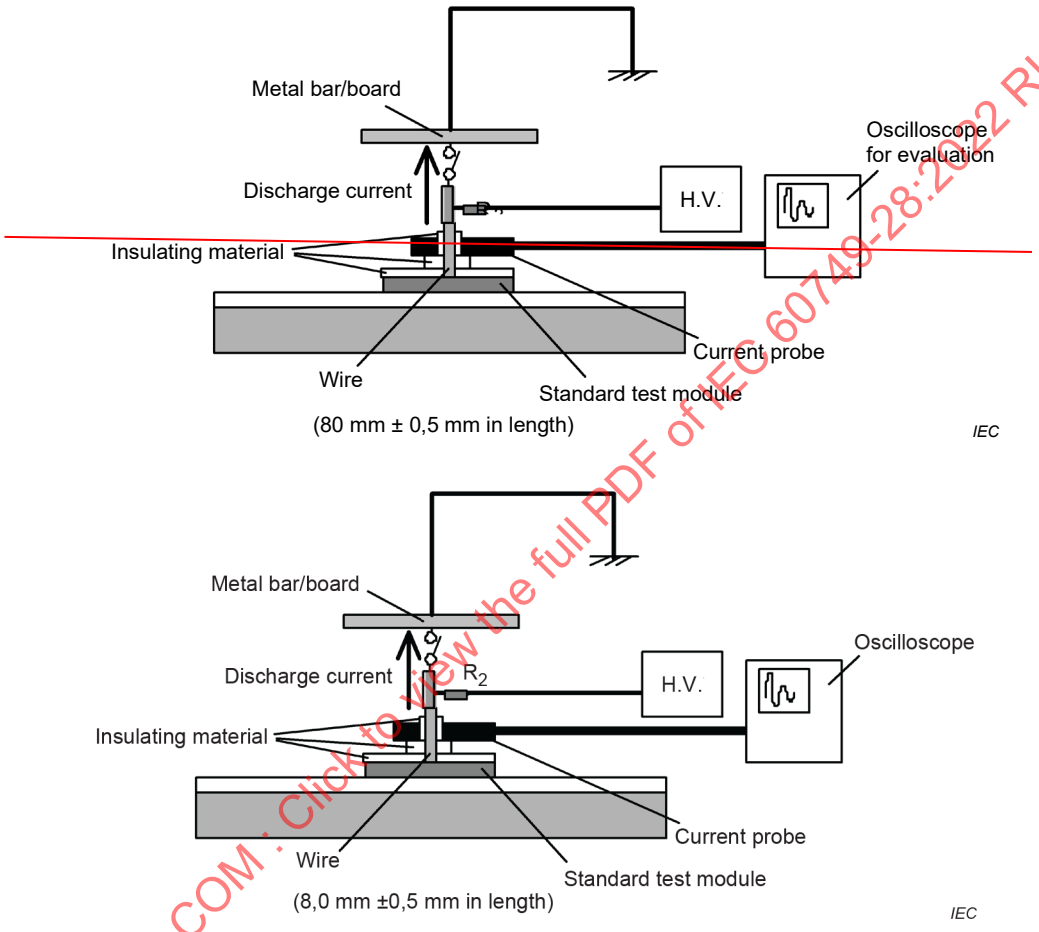


Figure J.4 – Measurement circuit for verification method using a current probe

J.4.3.2 Verification procedure

Verification is carried out as follows.

a) Clean the standard test modules and the insulating sheet using isopropanol.

b) Place the standard test module on the insulating sheet covering the metal plate. After passing a wire 8 mm in length through the hole for measurement of the current probe, the standard test module and the probe of the CDM equipment are connected to both ends of a wire, as shown in Figure J.4.

c) Apply a voltage to the standard test module. Unless otherwise specified, the voltages are +125 V, −125 V, +250 V, −250 V, +500 V, −500 V, +750V, −750V, +1 000 V and −1 000 V to meet the test voltage range. When a test exceeding 1 000 V is performed, a higher voltage such as 2 000 V is additionally applied.

d) The current waveform is measured with the current measurement circuit by closing the switch.

e) The value other than the peak current satisfies Figure J.3 and Figure J.2, and the peak current complies with Table J.4.

NOTE In the measuring method as shown in Figure J.4, the inclusion of an 8 mm wire spacer reduces the resultant peak current to the levels shown in Table J.4. A good correlation has been established using this method between the values in Table J.3 and Table J.4.

Table J.4 – Specification of peak current I_{p1} for the current probe verification method

Verification voltage (V)	Values of peak current I_{p1} (A)	
	Small standard test module	Large standard test module
125	0,9 to 1,3	1,7 to 2,6
250	1,8 to 2,6	3,5 to 5,2
500	3,6 to 5,2	7,0 to 10,3
750	5,4 to 7,8	10,5 to 15,5
1 000	7,3 to 10,4	14,0 to 20,6

J.5 Test procedure

J.5.1 Initial measurement

Complete DC parametric and functional testing are performed in accordance with the applicable device specification at ambient temperature, followed by testing at maximum operating temperature or the temperature required by the relevant specification.

J.5.2 Tests

Testing is performed as follows.

a) Place a DUT on the insulating sheet. The ambient temperature during testing is 25 °C ± 5 °C.

b) Connect all the terminals of the DUT to the resistive material R_3 if required in the relevant specification. Connect the electrode to the test terminal with the switch opened (see Figure J.1).

c) If the DUT has a special isolated structure where the whole DUT is not fully charged from the test terminal, connect all the terminals or all the power supply terminals of the DUT to the resistive material R_3 as shown in Figure J.1.

d) Set the high voltage power supply to the test voltage specified in the relevant specification.

e) Close the switch (see Figure J.1). Confirm the contact between the electrode/front end and the terminal of the DUT during the test.

f) Unless otherwise detailed in the relevant specification, one discharge is performed. When multiple discharges are to be made, repeat the instructions given in steps c) and d). However, there should be an interval of 0,1 s or more between discharges. Reverse the polarity of the testing voltage and perform steps d) to f) if it is detailed in the relevant specification.

g) Perform steps b) to f) for the next test terminal and repeat this procedure to test all the terminals.

h) Reverse the polarity of the testing voltage and perform steps b) to g). When step g) is completed, perform intermediate measurements or perform steps a) to g) on another DUT.

J.5.3 Intermediate and final measurement

Complete DC parametric and functional testing are performed in accordance with the applicable device specification at ambient temperature, followed by testing at maximum operating temperature or the temperature required by the relevant specification.

J.6 Failure criteria

The test is considered to have failed if, after exposure to ESD, the tested component no longer meets its data sheet specifications.

J.7 Classification criteria

All DUT should meet the test requirements of this document up to a particular voltage level in order for the part to be classified as meeting a particular sensitivity classification. Classification levels are shown in Table 3.

J.8 Summary

The following should be detailed in the relevant specification:

a) voltage used for verification (refer to J.4.3.2 c);
b) parameters and conditions of initial measurement (refer to J.5.1);
c) ambient temperature during test (when other than specified) (refer to J.5.2 a));
d) connection of the resistive material R3 to all terminals of DUT if needed (refer to J.5.2 b));
e) test voltage (refer to J.5.2 d));
f) number of samples to be tested (refer to J.5.1 and J.5.3);
g) number of discharges (when other than specified) (refer to J.5.2 f));
h) interval between repeated discharges (when other than specified) (refer to J.5.2 f));
i) procedures for reversing the testing voltage (when other than specified) (refer to J.5.2 f)) and J.5.2 h));
j) parameters and conditions of intermediate and final measurements (when other than specified) (refer to J.5.3).

Bibliography

IEC 60749-26, *Semiconductor devices – Mechanical and climatic test methods – Part 26: Electrostatic discharge (ESD) sensitivity testing – Human body model (HBM)*

IEC 60749-28

Edition 2.0 2022-03

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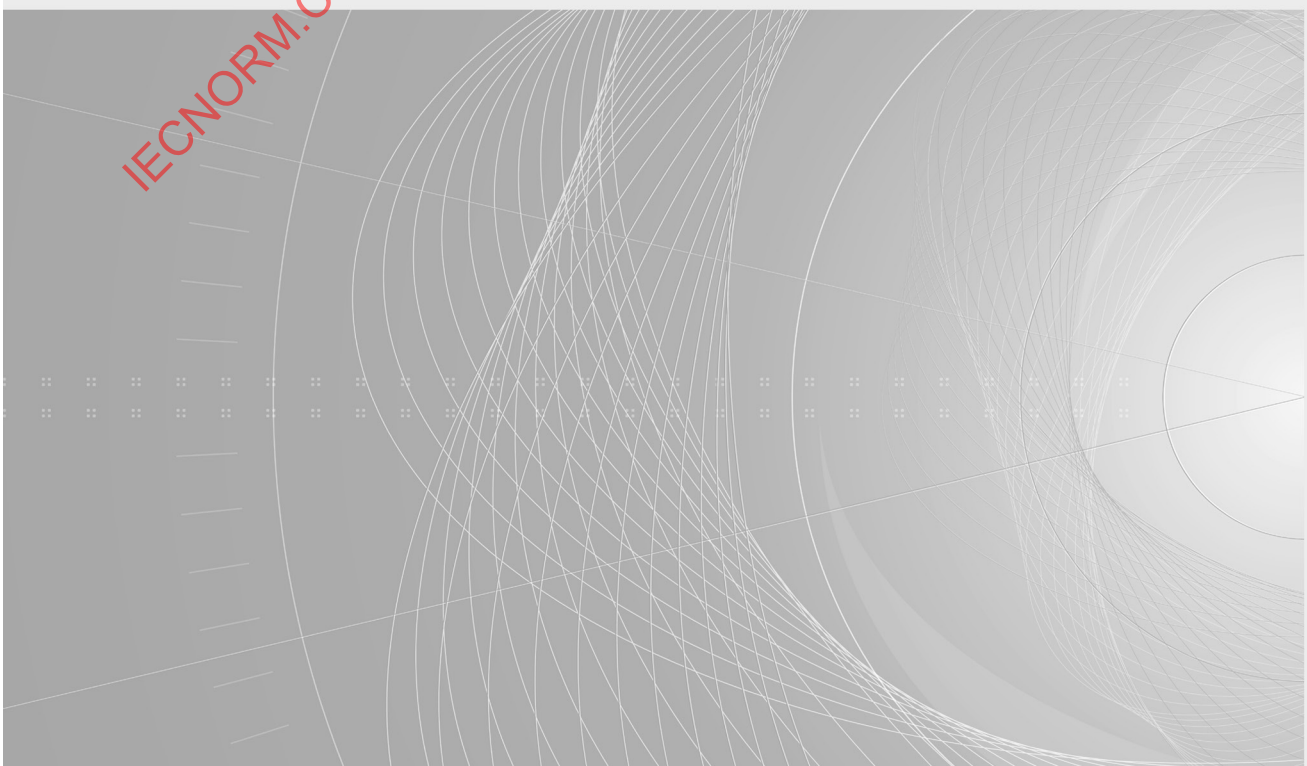
Semiconductor devices – Mechanical and climatic test methods – Part 28: Electrostatic discharge (ESD) sensitivity testing – Charged device model (CDM) – device level

Dispositifs à semiconducteurs – Méthodes d'essais mécaniques et climatiques – Partie 28: Essai de sensibilité aux décharges électrostatiques (DES) – Modèle de dispositif chargé (CDM) – niveau du dispositif



IEC 60749-28:2022-03(en-fr)

CONTENTS

INTERNATIONAL ELECTROTECHNICAL COMMISSION

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SEMICONDUCTOR DEVICES – MECHANICAL AND CLIMATIC TEST METHODS –

Part 28: Electrostatic discharge (ESD) sensitivity testing – Charged device model (CDM) – device level

FOREWORD

1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as "IEC Publication(s)"). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
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IEC 60749-28 has been prepared by IEC technical committee 47: Semiconductor devices, in collaboration with IEC technical committee 101: Electrostatics. It is an International Standard.

ANSI/ESDA/JEDEC JS-002-2018 has served as a basis for the elaboration of this standard. It is used with permission of the copyright holders, ESD Association and JEDEC Solid state Technology Association. ANSI/ESDA/JEDEC JS-002-2018 describes the field-induced (FI) method. An alternative, the direct contact (DC) method (not based on JS-002-2018), is described in Annex J.

This second edition cancels and replaces the first edition published in 2017. This edition constitutes a technical revision.

This edition includes the following significant technical changes with respect to the previous edition:

a) a new subclause and annex relating to the problems associated with CDM testing of integrated circuits and discrete semiconductors in very small packages;

b) changes to clarify cleaning of devices and testers.

The text of this International Standard is based on the following documents:

Draft	Report on voting
47/2746/FDIS	47/2754/RVD

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/standardsdev/publications.

A list of all parts in the IEC 60749 series, published under the general title *Semiconductor devices – Mechanical and climatic test methods*, can be found on the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

IMPORTANT – The 'colour inside' logo on the cover page of this publication indicates that it contains colours which are considered to be useful for the correct understanding of its contents. Users should therefore print this document using a colour printer.

INTRODUCTION

The earliest electrostatic discharge (ESD) test models and standards simulate a charged object approaching a device and discharging through the device. The most common example is IEC 60749-26, the human body model (HBM). However, with the increasing use of automated device handling systems, another potentially destructive discharge mechanism, the charged device model (CDM), becomes increasingly important. In the CDM, a device itself becomes charged (e.g. by sliding on a surface (tribocharging) or by electric field induction) and is rapidly discharged (by an ESD event) as it closely approaches a conductive object. A critical feature of the CDM is the metal-metal discharge, which results in a very rapid transfer of charge through an air breakdown arc. The CDM test method also simulates metal-metal discharges arising from other similar scenarios, such as the discharging of charged metal objects to devices at different potential.

Accurately quantifying and reproducing this fast metal-metal discharge event is very difficult, if not impossible, due to the limitations of the measuring equipment and its influence on the discharge event. The CDM discharge is generally completed in a few nanoseconds, and peak currents of tens of amperes have been observed. The peak current into the device will vary considerably depending on a large number of factors, including package type and parasitics. The typical failure mechanism observed in MOS devices for the CDM model is dielectric damage, although other damage has been noted.

The CDM charge voltage sensitivity of a given device is package dependent. For example, the same integrated circuit (IC) in a small area package can be less susceptible to CDM damage at a given voltage compared to that same IC in a package of the same type with a larger area. It has been shown that CDM damage susceptibility correlates better to peak current levels than charge voltage.

SEMICONDUCTOR DEVICES – MECHANICAL AND CLIMATIC TEST METHODS –

Part 28: Electrostatic discharge (ESD) sensitivity testing – Charged device model (CDM) – device level

1 Scope

This part of IEC 60749 establishes the procedure for testing, evaluating, and classifying devices and microcircuits according to their susceptibility (sensitivity) to damage or degradation by exposure to a defined field-induced charged device model (CDM) electrostatic discharge (ESD). All packaged semiconductor devices, thin film circuits, surface acoustic wave (SAW) devices, opto-electronic devices, hybrid integrated circuits (HICs), and multi-chip modules (MCMs) containing any of these devices are to be evaluated according to this document. To perform the tests, the devices are assembled into a package similar to that expected in the final application. This CDM document does not apply to socketed discharge model testers. This document describes the field-induced (FI) method. An alternative, the direct contact (DC) method, is described in Annex J.

The purpose of this document is to establish a test method that will replicate CDM failures and provide reliable, repeatable CDM ESD test results from tester to tester, regardless of device type. Repeatable data will allow accurate classifications and comparisons of CDM ESD sensitivity levels.

2 Normative references

There are no normative references in this document.

3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at http://www.electropedia.org/
- ISO Online browsing platform: available at http://www.iso.org/obp

3.1
CDM ESD
charged device model electrostatic discharge
electrostatic discharge (ESD) using the charged device model (CDM) to simulate the actual discharge event that occurs when a charged device is quickly discharged to another object at a lower electrostatic potential through a single pin or terminal

3.2
CDM ESD tester
charged device model electrostatic discharge tester
equipment that simulates the device level CDM ESD event using the non-socketed test method

Note 1 to entry: "Equipment" is referred to as "tester" in this document.

3.3
C_{Small}
device to CDM field plate capacitance for an integrated circuit or discrete semiconductor at or below which it has been determined that CDM testing is not required if specified conditions are met

3.4
dielectric layer
thin insulator placed atop the field plate used to separate the device from the field plate

3.5
field plate
conductive plate used to elevate the potential of the device under test (DUT) by capacitive coupling

Note 1 to entry: See Figure 1.

3.6
ground plane
conductive plate used to complete the circuitry for grounding/discharging the DUT

Note 1 to entry: See Figure 1.

3.7
software voltage
user/operator-entered voltage that, when combined with the scale factor or offset, sets the actual field plate voltage on the system in order to achieve the waveform parameters

Note 1 to entry: Waveform parameters are defined in Table 1 or Table 2.

3.8
test condition
TC
tester plate voltage that meets the waveform parameter conditions

Note 1 to entry: The waveform parameter conditions are found in a particular column of Table 1 and Table 2.

4 Required equipment

4.1 CDM ESD tester

4.1.1 General

Figure 1 represents the hardware schematic for a CDM tester setup to conduct field-induced CDM ESD testing assuming the use of a resistive current probe. The DUT may be an actual device or it may be one of the two verification modules (metal discs) described in Annex A. The pogo pin shall be connected to the ground plane with a 1 Ω current path with a minimum bandwidth (BW) of 9 gigahertz (GHz). The 1 Ω pogo pin to ground connection of the resistive current sensor may be a parallel combination of a 1 Ω resistor between the pogo pin and the ground plane, and the 50 Ω impedance of the oscilloscope and its coaxial cable. In Figure 1, K1 is the switch between charging the field plate and grounding the field plate. The CDM ESD testers used within the context of this document shall meet the waveform characteristics specified in Figure 2, and Table 1 and Table 2, without additional passive or active devices, such as ferrites, in the probe's assembly.

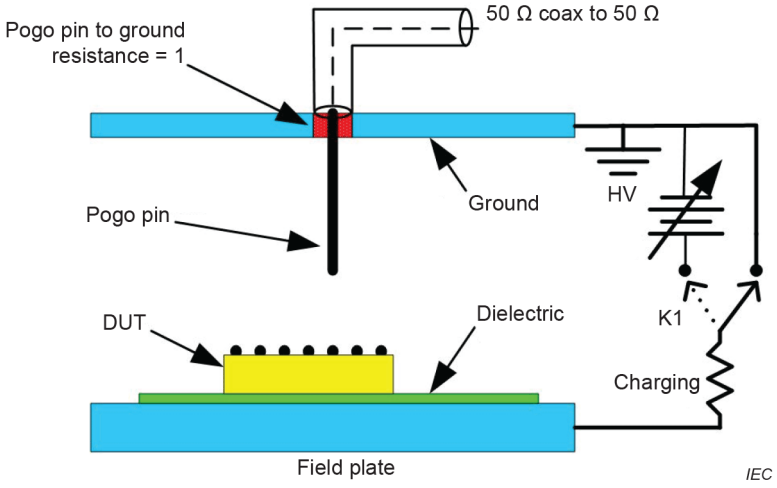


Figure 1 – Simplified CDM tester hardware schematic

When constructing the test equipment, the parasitics in the charge and discharge paths should be minimized since the resistance inductance-capacitance (RLC) parasitics in the equipment greatly influence the test results.

For existing equipment, it is recommended to contact qualified service personnel to determine compliance to this document upon removal of ferrite components.

4.1.2 Current-sensing element

A current-sensing element shall be incorporated into the ground plane. The resistance of this element shall have a value of (1,0 ± 10 %) Ω. A resistor, as specified in 4.1.1, shall be used as the current-sensing element. The value of resistance (including the 50 Ω cable/oscilloscope termination) shall be measured using an ohmmeter as described in 4.5. The resistance value shall be used to calculate the first peak current.

The current-sensing element shall have a minimum frequency response of 9 GHz (specified by a maximum roll-off of 3 dB at 9 GHz).

4.1.3 Ground plane

The probe assembly shall contain a square ground plane with the probe pin centred within it as shown in Figure 1. The dimensions of the ground plane shall be 63,5 mm × 63,5 mm ± 6,35 mm (2,5 inches × 2,5 inches ± 0,25 inches).

4.1.4 Field plate/field plate dielectric layer

The field plate shall have a surface flatness to vary no more than ± 0,127 mm (0,005 inches). The field plate dielectric layer should be made with an FR4 or similar epoxy-glass material. For FR4, the thickness and thickness tolerance of this dielectric layer should be 0,381 mm ± 0,0254 mm (0,015 inches ± 0,001 inches) in order to result in a capacitance measurement (as specified in normative Annex B) in the range specified in Table A.1.

If a different material is used, the material thickness is chosen to result in a capacitance measurement in the range specified in Table A.1.

4.1.5 Charging resistor

The charging resistor shown in Figure 1 shall nominally be 100 MΩ or greater.

Resistor values higher than 100 MΩ may be used, but this may not allow very large devices (refer to 5.9 and Annex I) to charge fully before being discharged by the probe assembly. This effect can be overcome by adding a delay between discharges in the CDM tester programming software. If using a resistor greater than 100 MΩ, it is recommended that the tester or the device itself be characterized to determine if a delay is needed for discharging large devices. A procedure for this large device delay characterization is given in Annex I.

4.2 Waveform measurement equipment

4.2.1 General

The CDM waveform measurement equipment shall consist of the following components.

4.2.2 Cable assemblies

Cable assemblies with combined internal tester cable and external cable total loss of no more than 2 dB at frequencies up to 5 GHz and a nominal 50 Ω impedance.

4.2.3 Equipment for high-bandwidth waveform measurement

4.2.3.1 High-bandwidth oscilloscope

An oscilloscope or transient digitizer with a minimum real-time (single shot) 3 dB BW of at least 6 GHz and ≥ 20 gigasample/s sampling rate with a nominal 50 Ω input impedance.

4.2.3.2 Attenuator

A 20 dB attenuator with a precision of ±0,5 dB, at least 12 GHz BW, and an impedance of 50 Ω ± 5,0 Ω.

4.2.4 Equipment for 1,0 GHz waveform measurement

4.2.4.1 1 GHz oscilloscope

An oscilloscope or transient digitizer with a real-time (single shot) 3 dB BW of 1 GHz with a nominal 50 Ω input impedance. The sampling rate shall be ≥ 5 gigasample/s.

NOTE The user has the option of using a higher BW oscilloscope and using a hardware or software filter to produce a bandwidth and sampling rate equivalent to that specified in 4.2.4.1.

4.2.4.2 Attenuator

A 20 dB attenuator with a precision of ± 0,5 dB, at least 4 GHz BW, and an impedance of 50 Ω ± 5 Ω.

4.3 Verification modules (metal discs)

The large verification module shall have a capacitance of (55 ± 5 %) pF and the small verification module shall have a capacitance of (6,8 ± 5 %) pF. Refer to normative Annex A for information on the verification module physical dimensions and normative Annex B for information on the capacitance measurement procedure.

4.4 Capacitance meter

Capacitance meter with a resolution of 0,2 pF, a measurement accuracy of 3 %, and a measurement frequency of 1,0 MHz as described in normative Annex B.

4.5 Ohmmeter

The ohmmeter used to measure the resistance of the resistive probe shall be capable of measuring to an accuracy of 0,01 Ω. Use of Kelvin 4-wire connections is recommended.

5 Periodic tester qualification, waveform records, and waveform verification requirements

5.1 Overview of required CDM tester evaluations

The CDM tester shall be qualified, re-qualified, and periodically verified as described in 5.5 and 5.6.

NOTE 1 Dielectric layers, ground planes (ground plates), the coaxial discharging resistor (probe), the distance between the ground plane and the field plate, the verification modules and the discharge contacts (e.g., pogo pins) are key elements of the tester construction. Any change to these elements necessitates a waveform verification.

NOTE 2 Changes in the shape of the discharge pulse, even though they can still be within specification, can indicate degradation of the discharge path.

5.2 Waveform capture hardware

Waveform capture requires the following instrumentation and tester set voltage procedure:

- an oscilloscope as specified in 4.2;
- an attenuator and cable assembly as defined in 4.2;
- verification modules (as described in 4.3) with the dimensions and attributes listed in normative Annex A and the method of measurement listed in normative Annex B.

5.3 Waveform capture setup

The waveform capture setup shall be carried out as follows:

a) Clean the verification modules. Avoid skin contact with the modules prior to, and during testing. A recommended procedure is described in normative Annex A.

b) Using an alcohol wipe, clean the discharge probe and the field charge plate on which the device is placed to remove any surface contamination that could result in charge loss. Ensure the pogo pin is free of particulates.

c) Attach the appropriate 20 dB attenuator as described in 4.2.3.2 to the oscilloscope. Attach one end of the external cable assembly, as described in 4.2.2, to the attenuator and the other end to the CDM tester. Verify all connections in the measurement chain are tight.

See informative Annex F for an example of oscilloscope settings and captured waveforms.

5.4 Waveform capture procedure

The waveform capture procedure shall be carried out as follows:

a) Place the verification module to be used on the field plate dielectric, ensuring intimate contact between the field plate dielectric and verification module.

b) Set the potential of the field plate to the needed voltage for the test condition being run.

c) Align the ground pin to approximately the centre of the verification module.

d) Either the single discharge or dual discharge method as described in Clause G.2 or Clause G.3 respectively can be used, but the discharge method chosen should be consistent with how products will be tested. When using the dual discharge method, waveforms for positive and negative pulses require a change in the oscilloscope trigger conditions to capture only positive or negative pulses.

e) Discharge the verification module at least ten times at the polarity being verified.

f) Observe at least ten successive waveforms during the set of discharges above and record the average waveform parameters for I_p, T_r, full width at half maximum (FWHM), and Ip2 for this group of waveforms as shown in Figure 2.

g) If the waveform characteristics do not meet the requirements as defined in either Table 1 or Table 2 for the target test condition (see 5.6 and 5.7 for the appropriate table and test conditions to use), re-clean the verification modules and ground pin, check that all connections are tight, make adjustments in the field plate voltage and repeat steps a) to g).

If this still does not work, check the system vacuum or look at replacement of the ground pin. Consult the tester manufacturer for more information.

Repeat the procedure for the opposite polarity.

5.5 CDM tester qualification/requalification procedure

5.5.1 CDM tester qualification/requalification procedure

The intent of the qualification/requalification procedure is to determine the field plate voltage needed for each test condition setting (125 to 1 000) in Table 3 to produce peak current in the ranges corresponding to Table 2, and therefore corresponding to the classification levels as specified in Table 3.

Two alternative procedures for how to qualify and routinely check the CDM test system are introduced in Annex H. These procedures are based on generally available CDM test systems and offer two methods for adjusting the field plate voltage to meet the waveform parameters of Table 2.

CDM test system manufacturers, or test system operators, may develop alternate qualification procedures from the two procedures in Annex H, as long as they result in waveforms that meet the requirements of Table 2 for the various test conditions.

It is recommended that settings determined from this qualification procedure be recorded for a particular test system, oscilloscope BW and polarity. This allows for detection of drift over time on the system, which may indicate a larger issue with the system. See Clause H.3 for examples.

Perform the setup and waveform capture steps as described in 5.3 and 5.5 under test conditions 125 to 1 000 in Table 2 for both positive and negative polarities using both small and large verification modules, and measuring with the high bandwidth oscilloscope as specified in 4.2.3.1. Refer to Annex H for example flowcharts of the procedures.

If local site test voltage ranges will always be narrower than the range above (for example test conditions 125 to 500), it is permissible to perform the qualification within that narrower range.

5.5.2 Conditions requiring CDM tester qualification/requalification

The CDM tester qualification and requalification as described in 5.5 is required in the following situations:

- acceptance testing when the CDM tester is delivered; usually performed by the manufacturer during installation;
- periodic requalification in accordance with the manufacturer's recommendations; the maximum time between requalification tests is one year;
- after service or repair that could affect the waveform.

5.5.3 1 GHz oscilloscope correlation with high bandwidth oscilloscope

During the first acceptance testing, the tester manufacturer shall use a high bandwidth oscilloscope as specified in 4.2.3.1 for initial waveform capture. If the test site only has a 1 GHz oscilloscope as specified in 4.2.4.1, the tester manufacturer and end user shall confirm using appropriate bandwidth filtering techniques and comparison with the oscilloscope from the tester manufacturer that the user's oscilloscope measures tester waveforms as defined in Table 1 for quarterly and routine waveform acceptance.

NOTE The Bessel-Thomson software filter option on many oscilloscopes is a suitable high-bandwidth waveform filter as it aligns well with actual 1 GHz oscilloscope data.

Oscilloscope correlation verification shall be repeated if the test site changes 1 GHz oscilloscopes.

5.6 CDM tester quarterly and routine waveform verification procedure

5.6.1 Quarterly waveform verification procedure

Perform the setup and waveform capture steps as described in 5.3 and 5.5 under test conditions 125 to 1000 in Table 1 using the 1 GHz oscilloscope as specified in 4.2.4.1 or Table 2 using the high-bandwidth oscilloscope as specified in 4.2.3.1. Both verification modules shall be checked at positive and negative polarities. Recommendation is to use the high bandwidth oscilloscope if the option exists. Refer to Annex H for example flowcharts of the procedures.

If local site test voltage ranges will always be narrower than the range above (for example test conditions 125 to 500), it is permissible to perform the qualification within that narrower range.

Tester waveform verification shall be performed at least once per quarter.

5.6.2 Routine waveform verification procedure

5.6.2.1 General

Perform the setup and waveform capture steps as described in 5.3 and 5.5 under test condition 500 in Table 1 (1 GHz oscilloscope) or Table 2 (high-bandwidth oscilloscope) for both positive and negative polarities using the verification module that most closely corresponds to the size package that will be tested. Refer to Annex H for example flowcharts of the procedures.

5.6.2.2 Routine verification frequency

Initially, upon tester qualification or requalification, routine waveform verification should be completed at least once per shift. If CDM stress testing is performed on consecutive shifts, waveform checks at the end of one shift may also serve as the initial check for the following shift.

Longer periods between routine waveform checks may be used if no changes in waveforms are observed for several consecutive checks. The test frequency and method chosen shall be documented. If, at any time, the waveforms no longer meet the specified limits, all ESD stress test data collected subsequent to the previous satisfactory waveform check shall be marked invalid and shall not be used for classification.

5.7 Waveform characteristics

The waveforms shall appear as shown in Figure 2 for both the positive polarity and its inverse for the negative polarity. The average waveform parameters (including I_p) as gathered by the method of 5.4 shall meet the specifications in Table 1 for a 1 GHz oscilloscope and Table 2 for a high-bandwidth oscilloscope. If a high-bandwidth oscilloscope is used for qualification, quarterly and routine waveform verifications, the 1 GHz requirements need not be considered.

Table 1 – CDM waveform characteristics for a 1 GHz bandwidth oscilloscope

1 GHz BW oscilloscope		**Test condition**									
		TC 125		TC 250		TC 500		TC 750		TC 1 000	
Verification module	Sym.	Small	Large	Small	Large	Small	Large	Small	Large	Small	Large
Peak current (A)	I_p	1,0 to 1,6	1,9 to 3,2	2,1 to 3,1	4,2 to 6,3	4,4 to 5,9	9,1 to 12,3	6,6 to 8,9	13,7 to 18,5	8,8 to 11,9	18,3 to 24,7
Rise time (ps)	t_r	< 350	< 450	< 350	< 450	< 350	< 450	< 350	< 450	< 350	< 450
Full width at half maximum (ps)	FWHM	325 to 725	500 to 1 000	325 to 725	500 to 1 000	325 to 725	500 to 1 000	325 to 725	500 to 1 000	325 to 725	500 to 1 000
Undershoot (A, max. 2nd peak)	I_{p2}	<70 % I_p	<50 % I_p	<70 % I_p	<50 % I_p	<70 % I_p	<50 % I_p	<70 % I_p	<50 % I_p	<70 % I_p	<50 % I_p

Table 2 – CDM waveform characteristics for a high-bandwidth (≥ 6 GHz) oscilloscope

≥ 6 GHz BW oscilloscope		**Test condition**									
		TC 125		TC 250		TC 500		TC 750		TC 1 000	
Verification Module	Sym.	Small	Large	Small	Large	Small	Large	Small	Large	Small	Large
Peak Current (A)	I_p	1,4 to 2,3	2,3 to 3,8	2,9 to 4,3	4,8 to 7,3	6,1 to 8,3	10,3 to13,9	9,2 to 12,4	15,5 to 20,9	12,2 to 16,5	20,6 to 27,9
Rise time (ps)	t_r	< 250	< 350	< 250	< 350	< 250	< 350	< 250	< 350	< 250	< 350
Full width at half maximum (ps)	FWHM	250 to 600	450 to 900	250 to 600	450 to 900	250 to 600	450 to 900	250 to 600	450 to 900	250 to 600	450 to 900
Undershoot (A, max. 2nd peak)	I_{p2}	<70 % I_p	<50 % I_p	<70 % I_p	<50 % I_p	<70 % I_p	<50 % I_p	<70 % I_p	<50 % I_p	<70 % I_p	<50 % I_p

NOTE The voltages of the test conditions 125 to 1 000 producing the specified peak current ranges are adjusted from previous classification test voltages of 125 V, 250 V, 500 V, 750 V and 1 000 V, respectively. Annex D describes this relationship between such voltages and ferrite-free tester set voltages. Tester adjusted field plate voltages to achieve these current ranges for the ferrite-free tester platform in this document can vary somewhat between testers. Annex H describes two voltage adjustment methods.

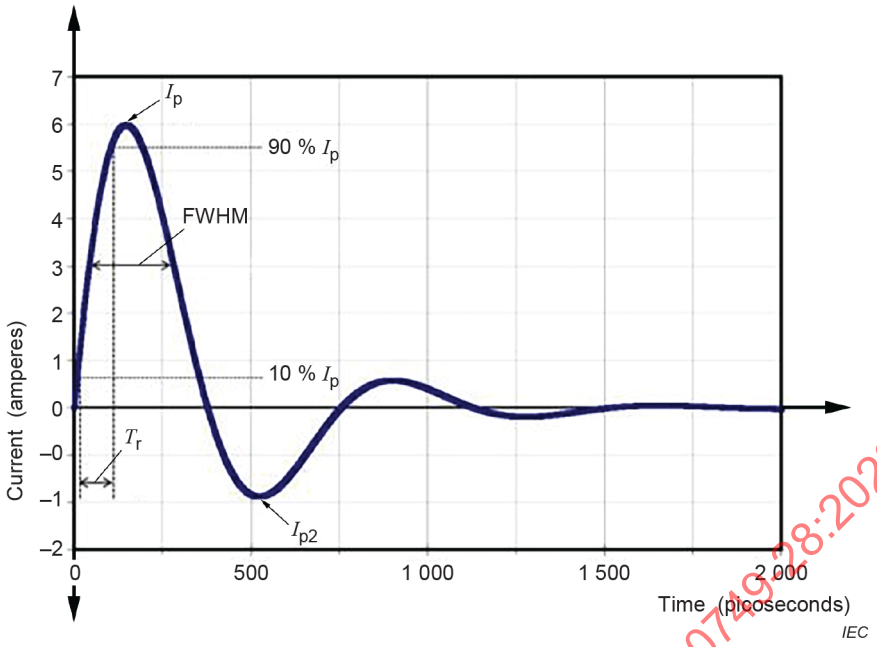


Figure 2 – CDM characteristic waveform and parameters

5.8 Documentation

Retain the waveform records for tester qualification according to internal company policy. For tester requalification, quarterly waveform verification and routine waveform verification, keep the records until the next set of waveforms are collected, or according to internal company policy.

5.9 Procedure for evaluating full CDM tester charging of a device

5.9.1 As defined in 4.1.5, the charging resistor should nominally be 100 MΩ or greater. If the resistor is too large, an added charging delay may be necessary to fully charge the device. To determine if an added delay is needed, follow the procedure in 5.9.2.

5.9.2 Using the large verification module, follow the procedure below.

a) Set the field plate voltage at +250 V (any voltage can be used as the objective is to monitor I_p).

b) With the pre- and post-charge delay both set to 0 ms, collect 10 waveforms and record the I_p from each. Calculate the average I_p of the waveforms.

c) With the pre-charge delay set to 500 ms (and post-charge delay remaining at 0 ms), collect ten waveforms, record the I_p from each. Calculate their average I_p of the waveforms.

d) Compare the average I_p value from the 0 ms charge delay and the 500 ms charge delay. If the average I_p is the same for both measurements, then a device of the same or lower capacitance as the large verification module are receiving a full charge. If the average I_p with 0 ms charge delay and 500 ms charge delay do not match, refer to the informative Annex I for a procedure to determine the appropriate default charge delay to add to the system.

e) Even if the two average I_p values above match, very large packaged devices (larger capacitance than the large verification module) may still require a delay in order to receive a full charge. Since device package technologies vary widely, there are no exact dimensions for how a particular package I_p may compare to the large verification module I_p for the evaluation described above.

f) To determine if a very large packaged device may still require a charge delay, steps a) to d) above can be repeated using the ground pin of a device. If the average I_p with 0 ms charge delay and 500 ms charge delay do not match, refer to the informative Annex I for a procedure to determine the appropriate charge delay.

In addition, where CDM testers have moving parts, care should be taken by personnel to avoid contact with these moving parts during operation.

6 CDM ESD testing requirements and procedures

6.1 Tester and device preparation

Devices used for CDM stressing shall not have been used for any prior stress tests.

ESD damage prevention procedures shall be used before, during, and after CDM and post parametric testing.

Devices shall be clean before testing. If needed, cleaning should be completed in compliance with company-approved procedures.

NOTE Isopropanol (isopropyl alcohol) is typically used for cleaning.

The CDM tester probe and field plate / dielectric shall be clean and dry before testing. Cleaning may be performed periodically or based on waveform acceptance using isopropanol (isopropyl alcohol) with a minimum isopropanol percentage of 70 %.

6.2 Test requirements

6.2.1 Test temperature and humidity

The test shall be carried out at room temperature. Humidity at the test head should not exceed 30 % RH. Heating or cooling the device during CDM testing is not intended.

The tester should be placed in an environment where the temperature is at room temperature.

NOTE Waveform repeatability is strongly dependent on moisture content of the air and having a low relative humidity will result in a more stable waveform.

6.2.2 Device test

6.2.2.1 Pre-stress testing

Prior to ESD stressing, complete static and dynamic testing shall be performed on all submitted devices. Parametric and functional results shall be within the limits specified in the datasheet parameters.

6.2.2.2 Failure criteria

Following ESD stressing, complete static and dynamic testing shall be performed on all stressed devices. A device is considered to have failed if parametric and functional test results are not within the limits specified in the datasheet parameters. A failure may be discounted if proven by failure analysis that it is not CDM–ESD related.

NOTE 1 A change in static leakage (e.g., pin leakage, standby current) is not an adequate criterion to determine pass/fail. It can serve as an indicator for the onset of damage.

NOTE 2 If testing is to be done at multiple temperatures, perform the test first at the lowest temperature, followed by increasing the temperature in sequence (e.g. −40 °C, +25 °C, +85 °C).

6.3 Test procedures

The test procedures are as follows.

a) Unless otherwise specified, obtain a minimum of three samples that have been verified to meet their data specifications.

b) CDM testing should begin at the lowest level in Table 3, but may begin at any level. However, if the initial voltage level is higher than the lowest level in Table 3 and the device fails at the initial voltage, testing shall be restarted with three fresh devices at the next lower level.

c) For each device, apply at least one positive and one negative discharge to each pin. Allow enough time (as specified in 5.9) between discharges for the device to reach the full test voltage level. Stresses may be partitioned by polarity, using a sample size of at least three units per polarity. Pins may also be partitioned into one or more sets of samples, provided that each pin of the device is a member of at least one set. Each set shall have a minimum of three units.

For the field-induced charging method, there are two possible procedures for charging and discharging the device: single and dual. Both procedures produce equivalent results. These procedures are described in the informative Annex G.

6.4 CDM test recording / reporting guidelines

6.4.1 CDM test recording

The CDM testing procedure for a particular product shall be recorded and stored per each company's data retention procedure. Information regarding tester waveform parameters should be available upon request; refer to Clause H.3 for more information on waveform parameter recording.

6.4.2 CDM Reporting Guidelines

Product CDM test results (including package information) shall be reported and be made available in the product reliability report.

For purposes of ensuring safe handling information for manufacturing control in an ESD protected area, it is highly recommended that publicly available product datasheets report CDM classifications.

6.5 Testing of Devices in Small Packages

Integrated circuits and discrete semiconductors (ICDS) in very small packages are very difficult to test for CDM and seldom fail CDM testing due to their small capacitance. It is not possible to specify a package dimension below which CDM testing is not needed as different technologies, design styles, and protection strategies have different susceptibilities to charged device events. In the absence of other information, all ICDS shall be tested. However, Annex C defines an optional procedure for establishing an integrated circuit capacitance C_{Small} for a specific technology and design flow. For devices with capacitance below C_{Small}, CDM testing is no longer required. ICDS with capacitance below C_{Small} and which satisfy the requirements of Annex C shall be considered to have a CDM passing level of TC 750 (Classification Level C2b in Table 3).

7 CDM classification criteria

ESD sensitive (ESDS) devices are classified according to the test procedure described in this document. CDM test results are specific to the particular package type used. The device classification is the highest ESD stress voltage level (both positive and negative polarities) at which a sample of at least three devices has passed full static and dynamic testing as per data sheet parameters following ESD testing. The CDM ESDS device classification levels are presented in Table 3.

Table 3 – CDM ESDS device classification levels

Classification level [a]	Classification test condition (in volts) [b]
C0a	< 125
C0b	125 to < 250
C1	250 to < 500
C2a	500 to < 750
C2b	750 to < 1 000
C3	≧ 1 000 [c]

[a] Use the "C" prefix to indicate a CDM classification level.

[b] The Classification Test Condition is not equivalent to the actual set voltage of the tester. See 5.6.1 and Annex H for further details.

[c] For test conditions above 1 000 V, depending on geometry of the device package, corona effects can limit the actual pre-discharge voltage and discharge current.

Annex A
(normative)

Verification module (metal disc) specifications and cleaning guidelines for verification modules and testers

A.1 Tester verification modules and field plate dielectric

The verification modules (metal discs) shall be made of brass, plated with nickel or gold/nickel, and may optionally have a gold flash coating over the nickel. They shall be manufactured to the dimensions specified in Table A.1 and shall be verified once before the initial use by either the manufacturer or user.

Caution shall be exercised during the manufacture of the discs so that they are free from burrs. If the perimeter of the disc has burrs, arcing may occur which may alter the results.

The field plate dielectric is chosen (see 4.1.4) to result in a capacitance measurement in the range specified in Table A.1.

Table A.1 – Specification for CDM tester verification modules (metal discs)

Disk	Small	Large
Diameter mm (inches)	8,89 ± 0,127 (0,350 ± 0,005)	25,4 ± 0,127 (1,000 ± 0,005)
Thickness mm (inches)	1,27 ± 0,05 (0,05 ± 0,002)	1,27 ± 0,05 (0,050 ± 0,002)
Surface flatness variation mm (inches)	≤ 0,127 (0,005)	≤ 0,127 (0,005)
Capacitance at 1 MHz (pF)	6,8 ± 5 %	55 ± 5 %

A.2 Care of verification modules

To avoid charge loss in verification modules during charged device model (CDM) evaluation, the verification modules should be cleaned using isopropanol (isopropyl alcohol, IPA) swabs for about 20 s as approved by the local safety organization, and dried in a moderate air stream to prevent charge leakage during test operation. Verification modules should be handled so as to maintain cleanliness.

The capacitance of the small and large verification modules (metal discs) shall be measured according to the procedure in Annex B, and shall conform to the values specified in Table A.1.

The tester should be cleaned periodically with isopropanol to remove any surface contamination that could result in charge loss. Particular attention should be paid to the discharge probe and field plate dielectric on which the device is placed.

Cleaning with isopropyl alcohol swabs can leave the surface moist for some period of time after the cleaning. The moisture can provide an unintended leakage path if present during the test. It is important to dry all surfaces after cleaning either by allowing sufficient time for the surfaces to dry or using forced air flow to evaporate the moisture.

Annex B
(normative)

Capacitance measurement of verification modules (metal discs) sitting on a tester field plate dielectric

a) The capacitance of the verification modules shall be measured in-situ (inside the CDM simulator), but can also be measured outside of the CDM simulator as guidance.

b) The small verification module is placed on the dielectric layer which is in direct contact with the surface of the grounded metallic field plate. Ensure there is no air space between the module and the dielectric layer, and also no air space between the dielectric layer and the metallic field plate. It is recommended that vacuum be used to ensure the verification module is held in place against the field plate dielectric.

c) Ensure the capacitance meter is "zeroed out" prior to measurement.

d) Connect the two leads from the capacitance meter (CP) as follows: One metallic lead/cable from the CP is connected to an exposed point on the field plate. The second metallic lead/cable from the CP is connected to the top of the verification module (in the centre). Measure the capacitance of the module to the grounded field plate. The capacitance value of the verification module shall be within the value specified in Table A.1.

e) Repeat steps a) to d) using the large verification module on the dielectric.

NOTE Placement of the CP meter leads can cause changes in the measured capacitance. One preventive technique for each verification module is to take a first measurement as outlined in item d)and then take a second measurement with the verification module lead/cable just above, but not touching, the verification module. The second reading is subtracted from the first to result in the true measured value.

It is recommended to use a meter with "guarded leads".

Annex C
(normative)

Testing of small package integrated circuits and discrete semiconductors (ICDS)

C.1 Testing rationale

This annex describes a procedure for setting a capacitance limit C_{small}, below which small package integrated circuits and discrete semiconductors no longer need to be tested for CDM. ICDS in very small packages are very difficult to test, due to the challenge of handling small devices. Very small ICDS also have very low capacitance to surroundings, including during CDM testing. With a small capacitance very little charge is transferred during a CDM event, either in a factory environment or during CDM testing. Small package ICDS therefore seldom fail during CDM testing. This does not, however, mean that there is no CDM risk for small package ICDS. The charge transferred during a small package CDM event can be small but the peak currents remain high, usually over an amp since the RLC equivalent circuit of a CDM event results in a very narrow, but still high current pulse. It is very difficult to set a minimum package dimension or capacitance for CDM testing because CDM failure levels depend on a wide variety of variables, including those listed below.

– capacitance between the ICDS and the field plate
– the technology used to fabricate the device
  - advanced low voltage technologies have thin gate oxides with low breakdown voltage and can be more susceptible to CDM damage without a proper protection scheme
  - high voltage technologies have diffusions which can be subject to CDM damage
– ESD protection circuits used in the device
– general ESD protection strategy used
– design style used to design the device
– thoroughness of ESD design rule checks
– package type which can influence inductance in the CDM current path

C.2 Procedure for Determining C_{small}

The following procedure can be used to determine a limit, C_{small} at and below which CDM testing is not required for a particular integrated circuit technology:

– Choose at least 5 ICDS designs from a technology, with varying package sizes
– The requirements for circuits to be considered from the same technology are given in C.3
– Measure the capacitance between each ICDS substrate, usually the ground pin, and the CDM tester's field plate when the ICDS is in the position for CDM testing, using the procedure in Annex B for measuring the capacitance of the verification modules.

Packages shall be at least 4 times the size of the vacuum hole in the dielectric layer or the metal field plate, whichever is larger. If the package is less than 4 times the size of the vacuum hole a test fixture which holds the package against the dielectric is used. At this time, there is no universally recognized method for testing CDM capability on packages that are less than 4 times the size of the vacuum holes. Techniques including mechanical methods for holding the package made of FR4 with the package not over vacuum holes, or packaging die in a different package, have been used.

– A separate test fixture can be used for measuring the capacitance if it uses the same thickness and material for the field plate dielectric layer as the CDM tester.
– Perform CDM testing at TC 1 000 for 3 samples in accordance with 6.3c) for each of the 5 ICDS designs.
– The ICDS capacitance, at which all ICDS with that capacitance and lower all pass CDM TC 1 000, is C_{small}.

To ensure there is no air space between the integrated circuit and the dielectric layer, and also no air space between the dielectric layer and the metallic field plate, the use of vacuum is recommended.

ICDS with substrate to CDM tester field plate capacitance equal to or less than C_{small} do not need to be tested for CDM if the following conditions are met:

– The ICDS has passed HBM according to requirements of the technology. This indicates the expected protection circuit is present.
– The ICDS uses the same technology, as defined in C.3, as used to determine C_{small}.
– ICDS devices not tested because their capacitance is below C_{small} and satisfy the above requirement shall be considered to have a CDM passing level of TC 750 (Classification Level C3b).

C.3 ICDS Technology requirements

ICDS are considered to be from the same technology if the following conditions are met:

- the ICDS shall use the same wafer fabrication flow.
- all ICDS shall use the same ESD protection circuits and ESD design rules.
- all ICDS shall have their substrate to CDM tester field plate capacitance measured using the procedures in Annex B.
- a separate test fixture which simulates the CDM tester field plate and dielectric can be used.
- calculated substrate to field plate capacitance can be used if the calculation procedure has been verified with measurements using the procedures in Annex B.

Annex D
(informative)

CDM test hardware and metrology improvements

The goal of this document is to reduce duplication of effort and confusion by developing a single agreed standard, correcting deficiencies in previous CDM standards whilst maintaining similar stress levels as those previous standards. This required significant hardware and metrology changes to arrive at an improved joint standard. This informative annex describes the motivations for these updates.

The major changes in this test method are listed below.

- Some details of the required waveforms have been modified to better match the high-frequency behaviour of CDM events.
- The test method now requires that the test head not include ferrites or other circuits to modify the high-frequency behaviour of the CDM pulse.
- The test method now requires that tester qualification and requalification be performed with a 6 GHz or faster oscilloscope, and recommends the use of 6 GHz or faster oscilloscopes for quarterly and regular tester verification if a fast oscilloscope is available.
- The tester qualification and verification procedures have been modified to give more flexibility in the field plate voltage settings to arrive at the required peak currents.
- The specification of test levels by voltage has been replaced by a series of test conditions which are related to the previous voltage levels.

When the original CDM test method was developed in the late 1980s, single-shot oscilloscopes with 1 GHz and higher bandwidths were expensive, not readily available and less capable than those available today. The result was that the original waveforms used to develop previous standards had a wider half-width than was characteristic of the actual CDM event. As measurement capability improved and the high frequency behaviour of test heads was improved, tester manufacturers found the peak width at half-height was narrower than allowed previously. In order to meet the peak width at half-height, ferrite beads were often added to the test head to bring the current waveforms into compliance. When oscilloscopes in the 4 GHz to 8 GHz range become readily available, it was found that the ferrite beads, which simply broadened the peak width when measured with a 1 GHz oscilloscope, created undesirable high-frequency harmonics with undesirable consequences. A primary goal in the development of this document was to remove the ferrite beads from the CDM test heads and to modify the waveform requirements to allow this change.

The 1 GHz oscilloscope specified previously is only marginally fast enough to capture CDM events and significantly reduces the measured peak current of the captured waveforms, especially for the small verification module and small integrated circuits. Accurate peak current measurements require the use of a measurement chain with 6 GHz or higher bandwidth, and the new joint standard reflects this requirement for CDM tester qualification. A 1 GHz oscilloscope was considered adequate for routine waveform verification, and that option is still available in the new standard, although the higher bandwidth oscilloscope is recommended if it is available.

The increased flexibility between the required peak current values and the field plate voltage to produce the peak current has been implemented for two reasons: to better match current practice, and to achieve similar stress levels as the legacy standards.

Previous standards specified the CDM tester geometry, as well as the required waveforms at specified field plate voltages. CDM tester manufacturers quickly found that it was often impossible to obtain the required peak current values with the required geometry and the specified field plate voltage. The manufacturers introduced adjustments to the field plate voltage so that the required waveforms were obtained when the specified voltage was selected in the CDM tester software. This adjustment was reasonable since it is known that it is peak current, not field plate voltage, which damages integrated circuits. The result was that when an integrated circuit passed 500 V, the field plate voltage was often considerably different than 500 V, but the intended current pulse was in fact applied to the device under test.

The removal of the ferrite beads, and the extra impedance which the beads produced, has resulted in higher peak currents than were present in legacy test methods for the same field plate voltage and tester geometry. This creates a second reason to give more flexibility in the setting of the field plate voltage to obtain the required peak currents. Since CDM failure is a result of the peak current during the CDM event, it is therefore more important that different CDM testers create the same peak current for specified test conditions rather than that the field plate voltages are the same. For this reason, the test voltages specified in the earlier standard CDM documents have been replaced by a series of test conditions producing peak currents similar to those at the specified voltages in recent previous standards.

Annex E
(informative)

CDM tester electrical schematic

Figure E.1 represents an electrical model of a CDM tester setup. CDUT is the capacitance between the DUT and the field plate, CDG is the capacitance between the DUT and the ground plane, and CFG is the capacitance between the field plate and the ground plane. The 1 Ω resistance between the pogo pin and the ground plane may be the parallel combination of the resistive probe and the coaxial cable/oscilloscope impedance as described above. The resistance of the spark which forms between the pogo pin and the DUT is assumed to be a variable resistance. The inductance of the pogo pin and spark are lumped together as a single inductor.

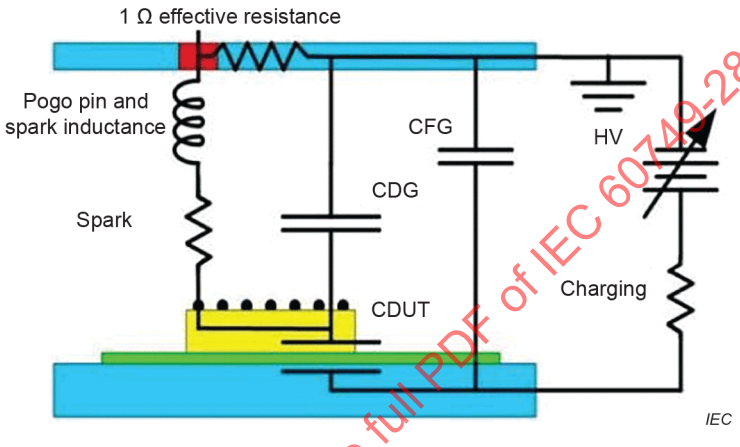


Figure E.1 – Simplified CDM tester electrical schematic

Annex F
(informative)

Sample oscilloscope setup and waveform

F.1 General

The following setup examples are based on measurements of a TC 500 waveform using a 1 GHz and 8 GHz oscilloscope. Other oscilloscopes will have different settings, but this annex should provide basic guidelines that can be used on most oscilloscopes.

F.2 Settings for the 1 GHz bandwidth oscilloscope

Vertical	200 mV/division (small verification module) or 200 mV/division (large verification module)
Timebase	400 ps/division
Trigger	300 mV small verification module or 400 mV large verification module
Impedance	50 Ω

These settings are for an oscilloscope for which the attenuation correction could not be made.

F.3 Settings for the high-bandwidth oscilloscope

Vertical	2 V/division (small verification module) or 2 V/division (large verification module)
Timebase	400 ps/division
Trigger	3 V small verification module or 4 V large verification module
Impedance	50 Ω

These settings are for an oscilloscope for which the attenuation correction was made in the oscilloscope software.

F.4 Setup

Attach the 20 dB attenuator to the oscilloscope. Attach the cable to the end of the attenuator and to the voltage output of the CDM tester.

NOTE The 20 dB attenuator is a 10× attenuator. If the oscilloscope does not automatically compensate for this, the measurements need to be multiplied by 10 to get the correct reading (e.g. from the small verification module used in figure F.1, 532 mV = 5,32 A peak current).

F.5 Sample waveforms from a 1 GHz oscilloscope

Sample waveforms from a 1 GHz oscilloscope are illustrated in Figure F.1 and Figure F.2.

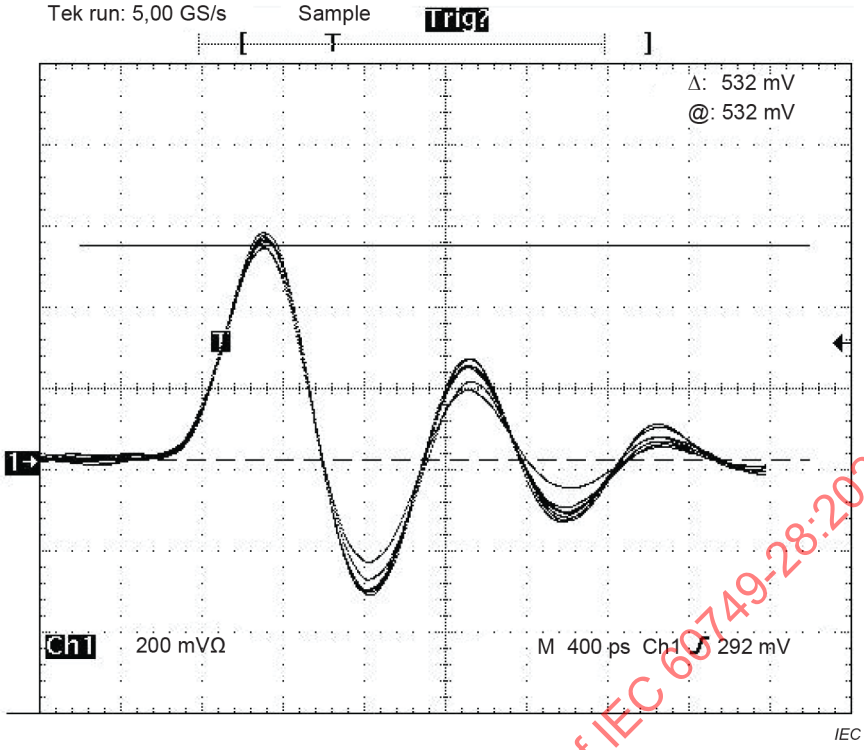


Figure F.1 – 1 GHz TC 500, small verification module

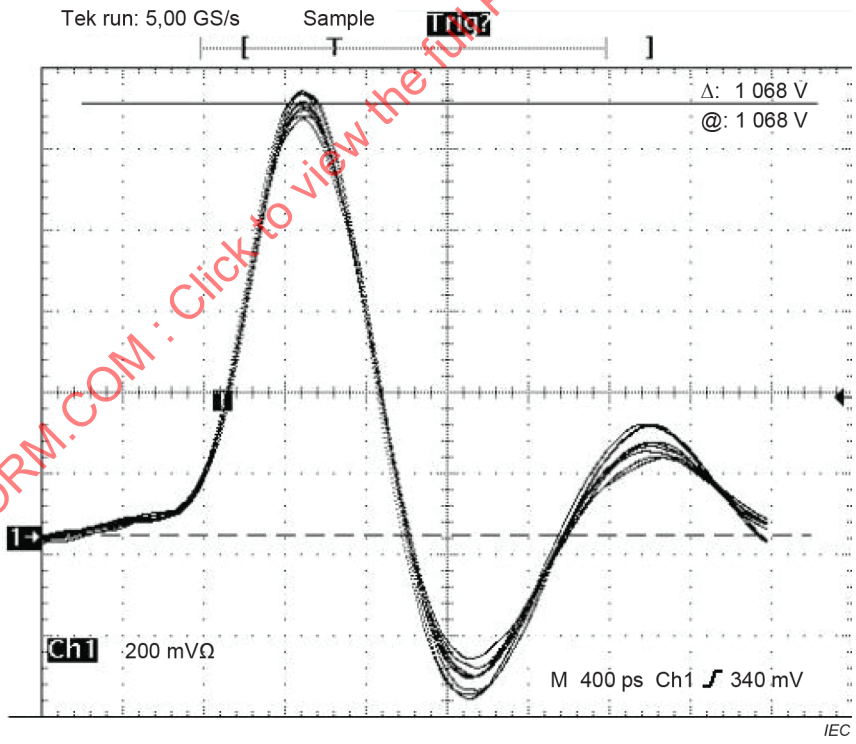


Figure F.2 – 1 GHz TC 500, large verification module

F.6 Sample waveforms from an 8 GHz oscilloscope

Sample waveforms from an 8 GHz oscilloscope are illustrated in Figure F.3 and Figure F.4.

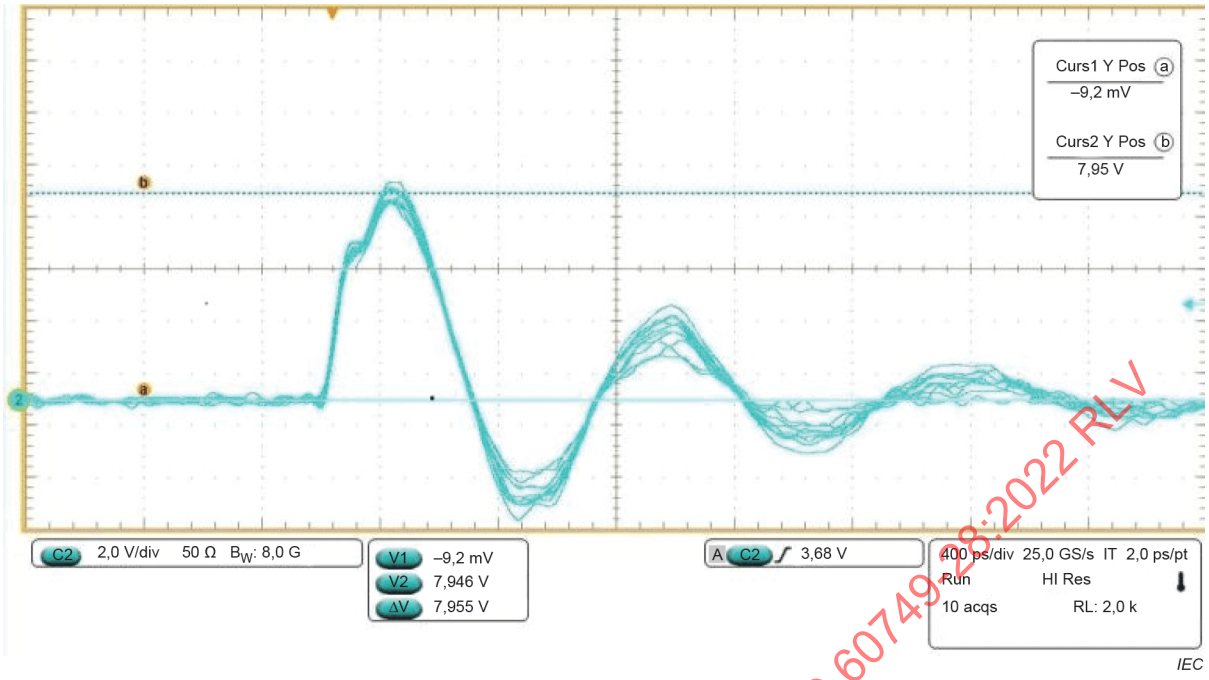


Figure F.3 – 8 GHz TC 500, small verification module (oscilloscope adjusts for attenuation)

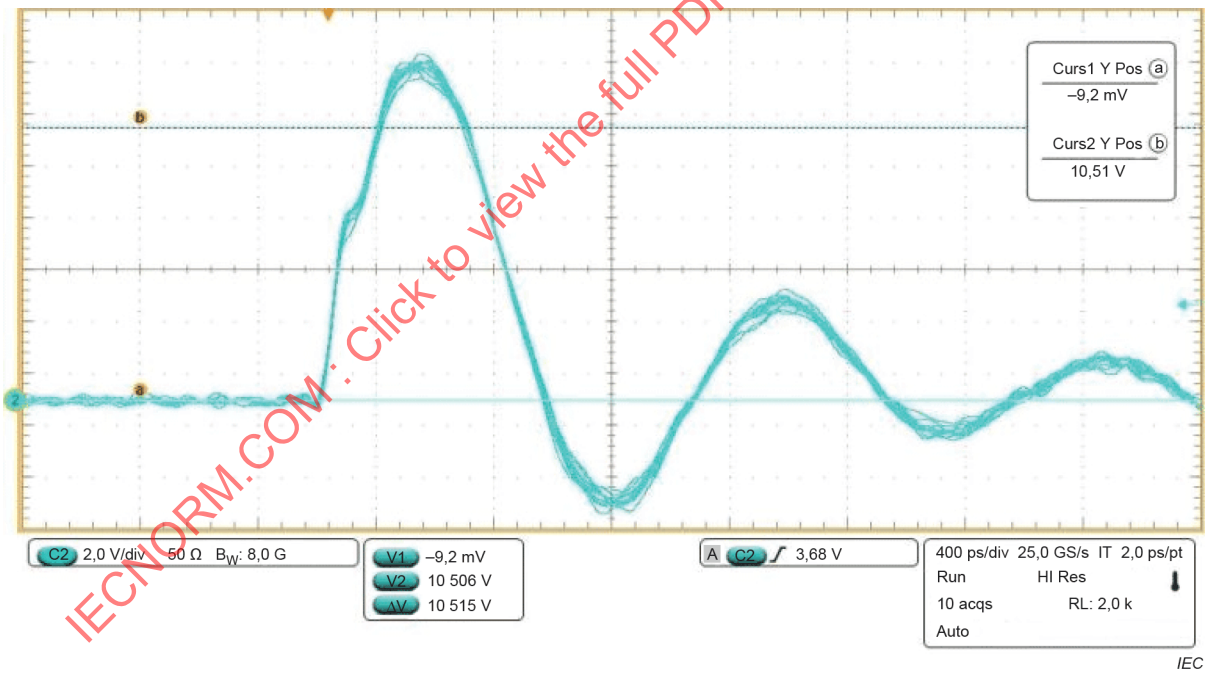


Figure F.4 – GHz TC 500, large verification module (oscilloscope adjusts for attenuation)

Annex G
(informative)

Field-induced CDM tester discharge procedures

G.1 General

Annex G describes the two types of discharge procedures used in field-induced CDM test equipment.

G.2 Single discharge procedure

The single positive and single negative discharges can be applied with two individual discharges using this sequence of steps producing the sequence of charging/discharging events as illustrated in Figure G.1.

a) Place the uncharged DUT on the field plate and align it.

b) The field voltage is established by raising the voltage on the field plate to the specified stress level.

c) The first discharge is made by lowering the pogo pin to the DUT (see Figure G.1).

d) The pogo pin continues to descend until it makes physical contact with the device pin under test (PUT) to ensure full charge transfer and to provide a conduction path to ground.

e) Then the voltage on the field plate is slowly (resistively) returned to zero, which completely removes the charge that was transferred to the DUT during the first CDM discharge.

f) The pogo pin is returned to its starting (separated) position (see Figure G.1) before the voltage of the same or opposite polarity is applied to the field plate for subsequent discharges.

g) Repeat for each pin to be tested.

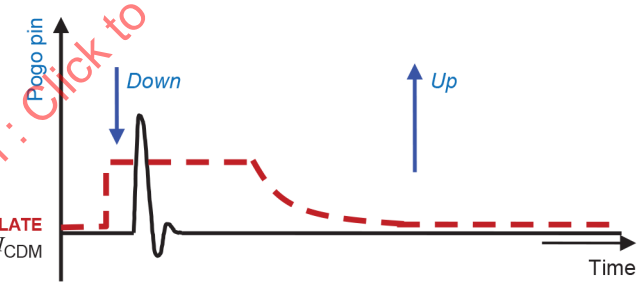


Figure G.1 – Single discharge procedure (field charging, I_{CDM} Pulse, and slow discharge)

G.3 Dual discharge procedure

The single positive and single negative discharges can be applied with one pair of alternating polarity discharges using this sequence of steps producing the sequence of charging/discharging events as illustrated in Figure G.2.

a) Place the uncharged DUT on the field plate and align it.

b) The field voltage for the positive stress is established by raising the voltage on the field plate to the specified stress level.

c) The first discharge is made by lowering the pogo pin to the DUT (see Figure G.2).

d) The pogo pin continues to descend until it makes physical contact with the DUT. This is to ensure full charge transfer and to provide a conduction path to ground.

e) The pogo pin is returned to its starting separated position (see Figure G.2), leaving the device with a net charge.

f) The voltage on the field plate is slowly (resistively) returned to zero, which completely removes the charge on the field plate. The DUT will still have a net charge.

g) The pogo pin is lowered (the second down arrow to the right in Figure G.2) a second time for the second discharge, which will be of opposite polarity and the same magnitude.

h) Repeat for each pin to be tested.

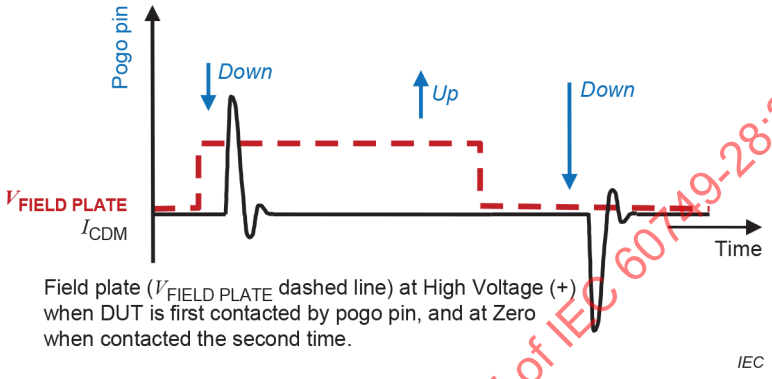


Figure G.2 – Dual discharge procedure (field charging, 1st I_{CDM} pulse, no field, 2nd I_{CDM} pulse)

Annex H
(informative)

Waveform verification procedures

H.1 Factor/offset adjustment method

This procedure aligns the tester for direct software voltage input of the test condition for the full alignment range. This method may not allow for alignment of each test condition with the target mid-range of I_p as shown in Table 1 or Table 2, but it is the easiest to use in a lab environment with multiple testers, as the software voltage entered matches the test condition target level and does not require linear interpolation/extrapolation for test conditions other than the five levels listed in Table 1 or Table 2.

The requirements/details of this method are as follows:

– a single factor/offset is used across the entire test condition range;
– a different factor/offset can be used for each polarity;
– the same factor/offset shall be used for both large and small verification modules.

Figure H.1 below depicts the waveform verification flow for qualification/re-qualification and quarterly checks, while Figure H.2 shows the flow for routine verifications. Table H.1 shows an example of the data that should be recorded.

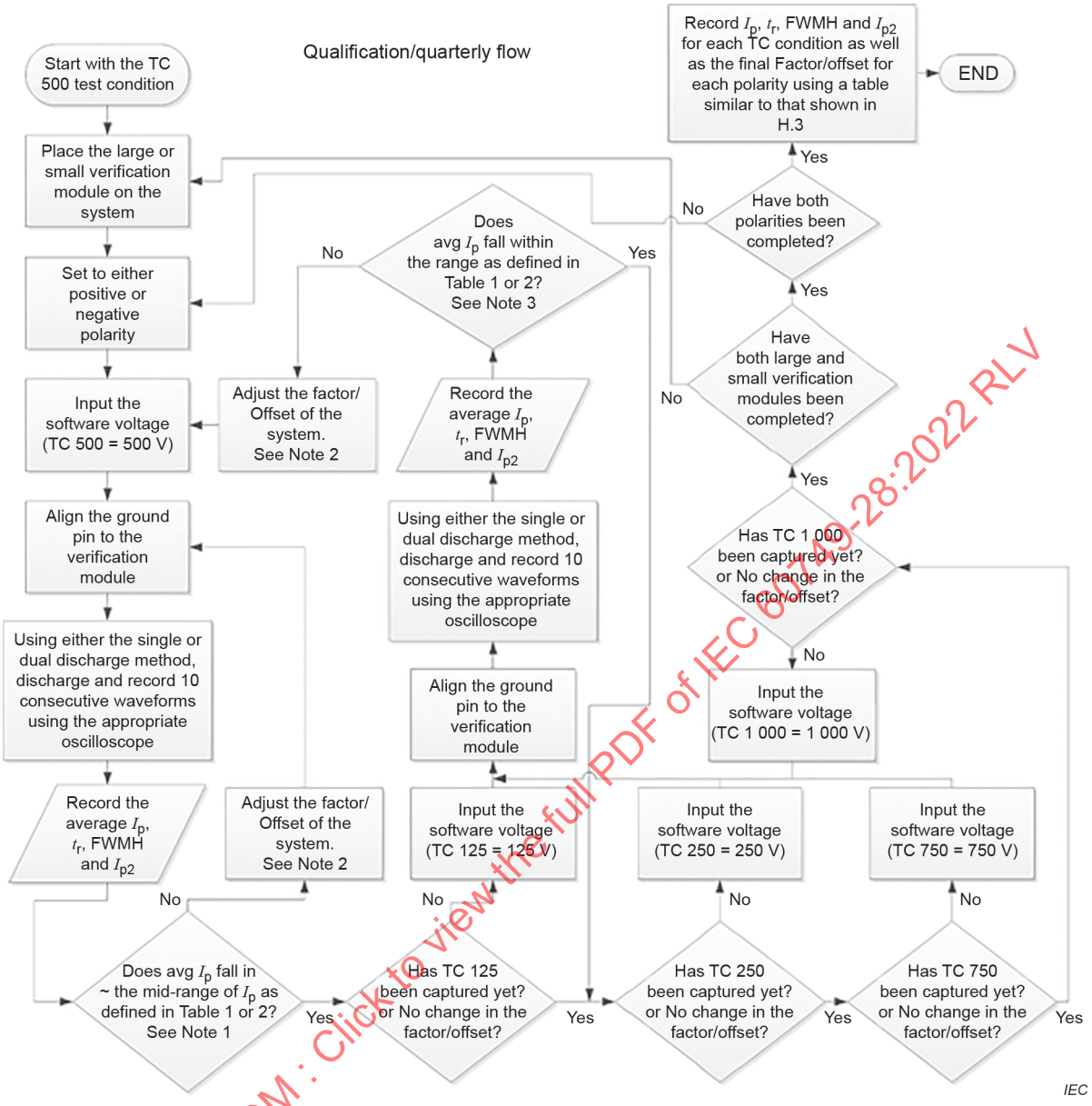


Figure H.1 – An example of a waveform verification flow for qualification and quarterly checks using the factor/offset adjustment method

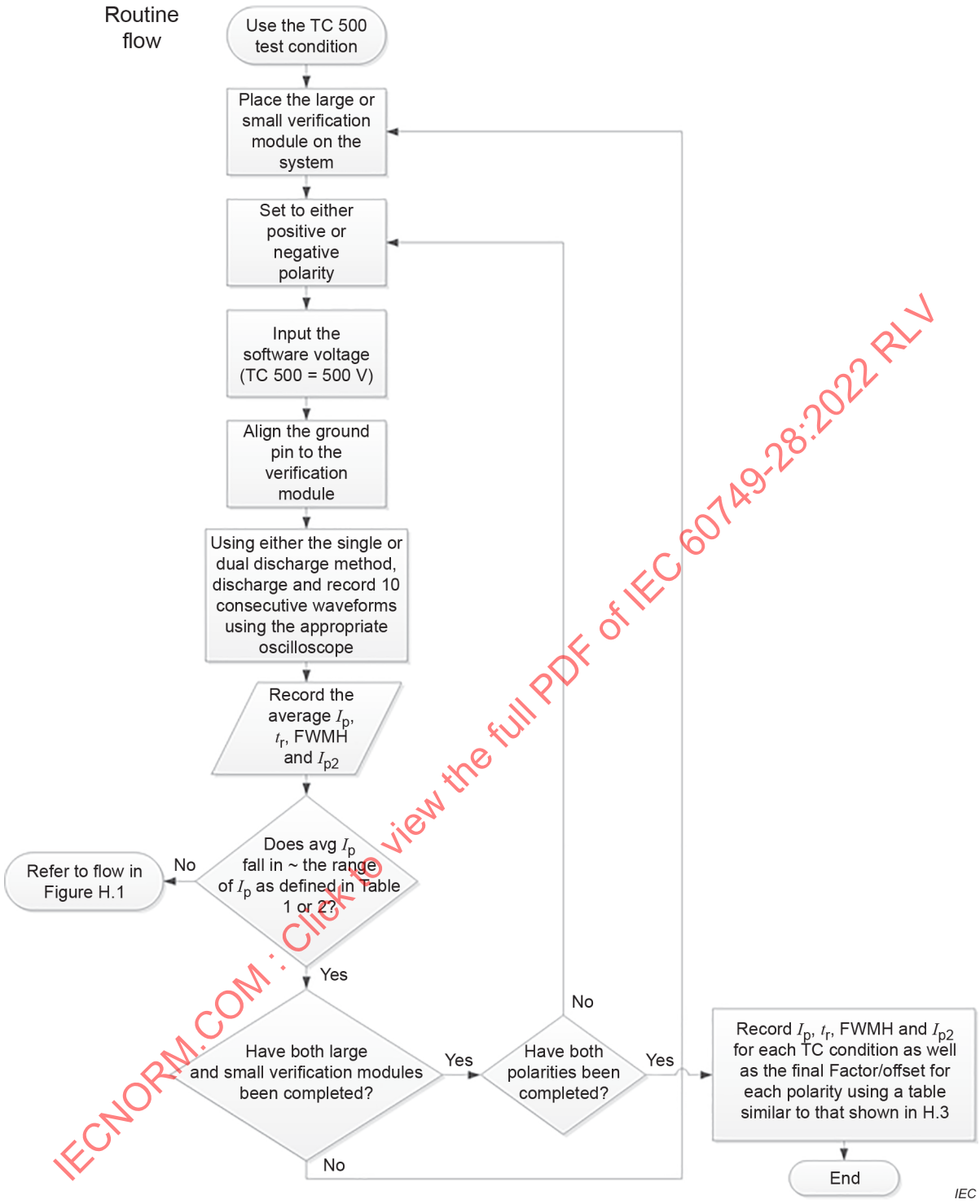


Figure H.2 – An example of a waveform verification flow for the routine checks using the factor/offset adjustment method

NOTE 1 Targeting to the mid-range of TC 500 is a starting point for adjustment of the field plate voltage. Based on the results of the other test conditions (TC 125/250/750/1 000) the I_{peak} can end up higher or lower than the mid-range value on TC 500. As shown in Figure H.3, adjustments in the factor/offset can shift the I_{peak} higher or lower.

NOTE 2 To properly calibrate systems, tester manufacturers have implemented a secondary "adjustment" parameter as an offset from the software voltage setting, either represented as a voltage "multiplier" value or a percentage "offset" value which modifies the field plate voltage. The tester manufacturer can be consulted for more detail.

After several iterations through this loop, if the user finds they cannot meet the I_{peak} range as defined in Table 1 or Table 2 or the factor/offset is outside the typical documented range, the verification modules and ground pin can be cleaned and all connections checked for tightness. If this still does not work, the system vacuum can be checked or the ground pin replaced. The tester manufacturer can be contacted for more information.

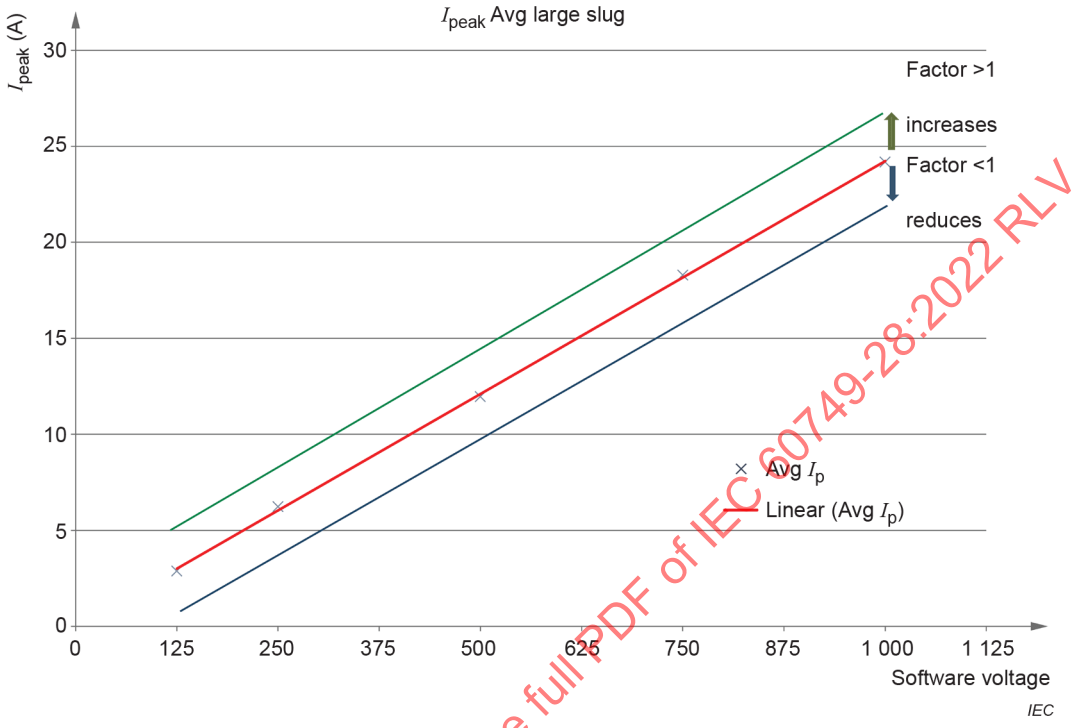


Figure H.3 – Example of average I_{peak} for the large verification module – high bandwidth oscilloscope

H.2 Software voltage adjustment method

This procedure does not adjust the factor/offset but leaves the factor/offset with a value that will not impact the field plate voltage and uses the software voltage entry as the primary adjustment of the field plate voltage. This method will allow for a much more accurate targeting of the midpoint of the I_p range as defined in Table 1 or Table 2, but creates complexity in determining the correct software voltage entry between the five test conditions. Determining software voltage entries, other than the five test condition levels, (which will be determined in this procedure) will require linear interpolation/extrapolation.

The requirements/details of this method are as follows:

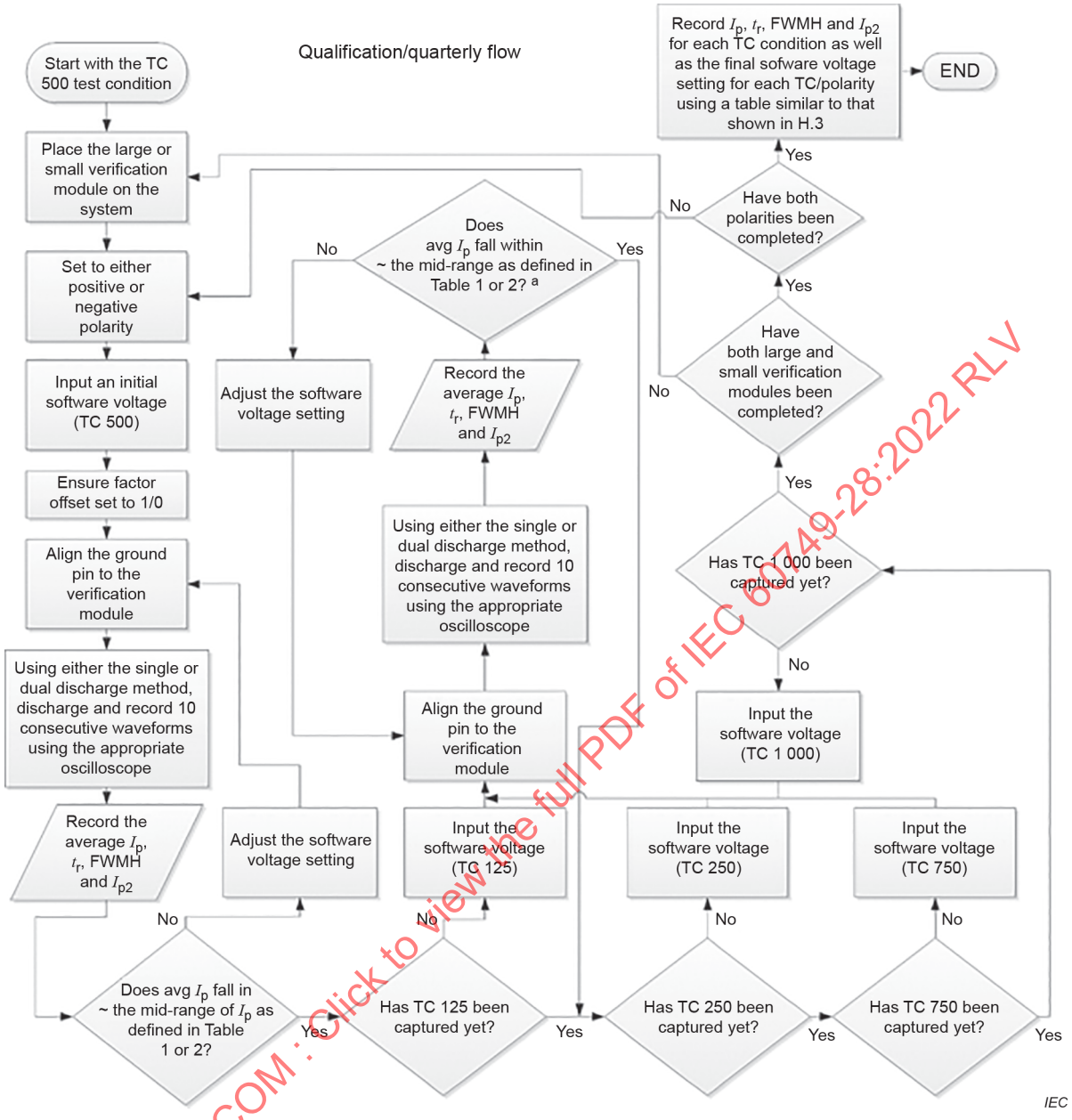
– a unique software voltage setting is determined for each test condition;

– unique voltage settings may be used for each polarity (at each test condition);

– the same software voltage setting shall be used for both large and small verification modules at each test condition;

– testing at levels other than the five test conditions will require a linear interpolation/extrapolation to determine the correct software voltage entry.

Figure H.4 below depicts the waveform verification flow for qualification/re-qualification and quarterly checks while Figure H.5 shows the flow for routine verifications. Table H.2 shows an example of the data which should be recorded.



a After several iterations through this loop, if the user finds they cannot meet the I_{peak} range as defined in Table 1 or Table 2 or that the software voltage setting is well outside the typical documented range, re-clean the verification modules and ground pin and check that all connections are tight. If this still does not work, check the system vacuum or look at replacement of the ground pin. Consult the tester manufacturer for more information.

Figure H.4 – An example of a waveform verification flow for qualification and quarterly checks using the software voltage adjustment method

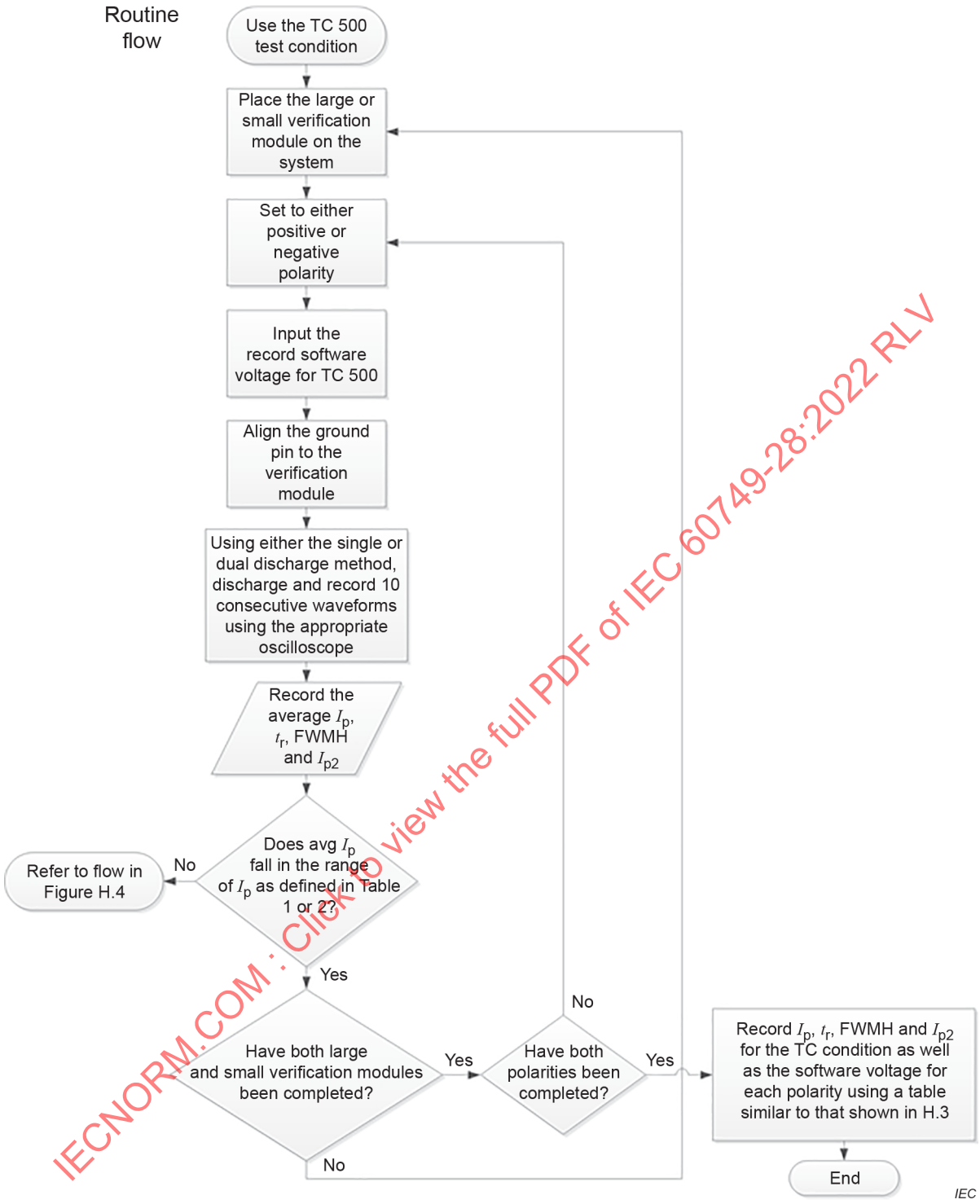


Figure H.5 – An example of a waveform verification flow for the routine checks using the software voltage adjustment method

H.3 Example parameter recording tables

Table H.1 gives an example table of CDM qualification/quarterly verification waveform parameters to be recorded for the factor/offset adjustment method.

Table H.1 – Example waveform parameter recording table for the factor/offset adjustment method

Tester – System # 1									
Polarity = positive		Scope bandwidth = 8 GHz				Factor/offset final setting = 0,82			
Module size	Date	% RH	Test cond	Software voltage	$I_{P\ AVG}$ (A)	$t_{R\ AVG}$ (ps)	FWHM $_{AVG}$ (ps)	$I_{P2\ AVG}$ (A)	I_{P2} (% I_{P1})
Large	dd/m/yy	*X* %	TC 500	500	12,1	275	610	4,3	36 %
Small	dd/m/yy	*X* %	TC 500	500	7,30	185	400	3,7	51 %
Large	dd/m/yy	*X* %	TC 125	125	2,90	283	611	1,1	38 %
Small	dd/m/yy	*X* %	TC 125	125	1,90	201	395	1,1	58 %
Large	dd/m/yy	*X* %	TC 250	250	6,00	276	609	2,2	37 %
Small	dd/m/yy	*X* %	TC 250	250	3,70	186	397	2,1	57 %
Large	dd/m/yy	*X* %	TC 750	750	18,30	274	611	7,2	39 %
Small	dd/m/yy	*X* %	TC 750	750	11,00	190	398	6,1	55 %
Large	dd/m/yy	*X* %	TC 1 000	1 000	24,40	276	612	9,2	38 %
Small	dd/m/yy	*X* %	TC 1 000	1 000	14,60	187	399	7,4	51 %

Table H.2 gives an example of CDM qualification / quarterly verification waveform parameters to be recorded for the software voltage adjustment method.

Table H.2 – Example waveform parameter recording table for the software voltage adjustment method

Tester – System # 2									
Polarity = positive		Scope bandwidth = 8 GHz				Factor/offset final setting = 1/0			
Module size	Date	% RH	Test cond	Software voltage	$I_{P\ AVG}$ (A)	$t_{R\ AVG}$ (ps)	FWHM $_{AVG}$ (ps)	$I_{P2\ AVG}$ (A)	I_{P2} (% I_{P1})
Large	dd/m/yy	*X* %	TC 500	410	12,1	275	610	4,3	36 %
Small	dd/m/yy	*X* %	TC 500	410	7,30	185	400	3,7	51 %
Large	dd/m/yy	*X* %	TC 125	105	2,90	283	611	1,1	38 %
Small	dd/m/yy	*X* %	TC 125	105	1,90	201	395	1,1	58 %
Large	dd/m/yy	*X* %	TC 250	205	6,00	276	609	2,2	37 %
Small	dd/m/yy	*X* %	TC 250	205	3,70	186	397	2,1	57 %
Large	dd/m/yy	*X* %	TC 750	620	18,30	274	611	7,2	39 %
Small	dd/m/yy	*X* %	TC 750	620	11,00	190	398	6,1	55 %
Large	dd/m/yy	*X* %	TC 1 000	840	24,40	276	612	9,2	38 %
Small	dd/m/yy	*X* %	TC 1 000	840	14,60	187	399	7,4	51 %

Annex I
(informative)

Determining the appropriate charge delay for full charging of a large module or device

I.1 General

Annex I describes the procedure for characterizing the charge delay on the CDM tester and determining the appropriate delay (for full charging) as either the default delay for the system (if the initial large verification module checkout fails as described in 5.9) or the delay required for a very large package device.

I.2 Procedure for charge delay determination

Follow the procedure below to determine an appropriate charge delay.

Using the large verification module or the ground pin of a very large package device:

a) Set the field plate voltage at +250 V (any voltage can be used as the objective is to monitor I_p).

b) With the pre-/post-charge delay set to 0 ms, collect 10 waveforms and record the I_p from each. Calculate the average I_p of the waveforms.

c) Increase the pre-charge delay by 50 ms, collect 10 waveforms, record the I_p from each, and calculate their average I_p.

d) Continue incrementing the delay by 50 ms (a larger or smaller step can be chosen) and record the average I_p until a minimum of 500 ms charge delay.

e) Plot the results as shown in Figure I.1.

f) The appropriate charge delay results in a "saturation point" for I_p. As shown in Figure I.1, I_p for this example saturates at ~300 ms. Adding some guard band to this example would ensure that a pre-charge delay of 400 ms would be sufficient as either the default charge delay on the system (if the large verification module had been used) or as the required charge delay on a specific large package device if a large device had been used as the vehicle for the data collection.

g) For most large devices, it is expected that 500 ms will be sufficient to reach a saturation point. However, if after 500 ms, a saturation point has not been reached, repeat steps d) and e) until this occurs.

h) It is important to note that longer delay times do not "overcharge" the device but would only increase test time.

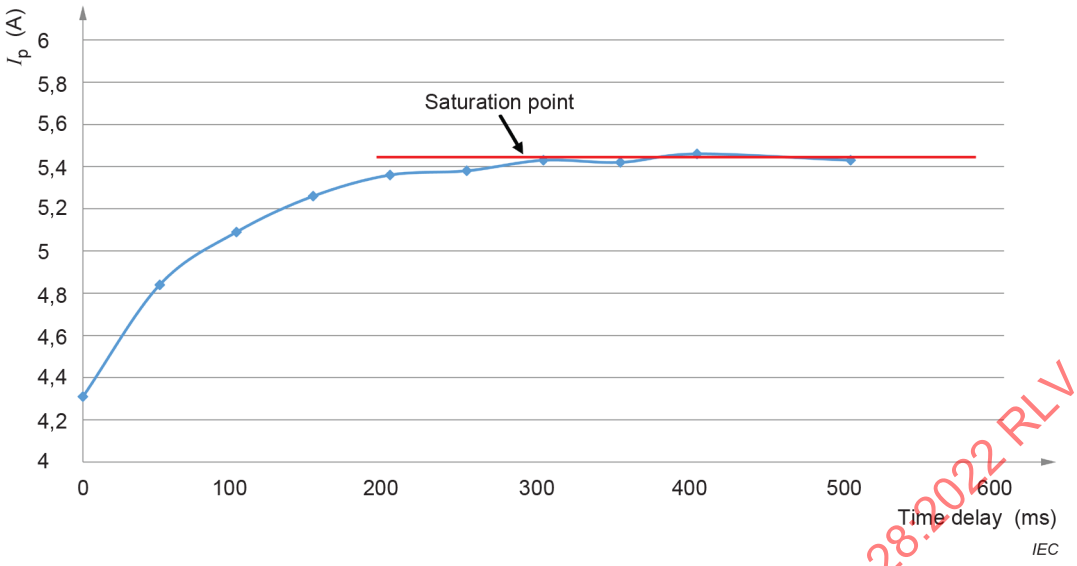


Figure I.1 – An example characterization of charge delay vs. I_p

Annex J
(informative)

Electrostatic discharge (ESD) sensitivity testing direct contact charged device model (DC-CDM)

NOTE The method identified in Annex J has not been shown to give results that correlate with results using the hardware and field-induced method specified in the body of this document.

J.1 General

Annex J describes the direct contact charged device model (DC-CDM) for the electrostatic discharge test method, which is used to evaluate the sensitivity of integrated circuits to electrostatic discharges. It is an alternative to the field-induced (FI) model.

This test method is used to reproduce and evaluate the effect of the discharge of a device.

This test method is for use on packaged devices. Where it is necessary to evaluate components that are shipped as wafers or bare chips, the components are assembled into a package similar to that expected in the final application.

This test method is classified as destructive.

J.2 Standard test module

Two types of the metal disks (listed in Table J.1), one small and one large, are used as the standard test modules, and are made of brass plated with nickel or gold/nickel and may optionally have a gold flash coating over the nickel.

The standard test modules for the field-induced CDM simulator can be cleaned in an ultrasonic bath using isopropanol for about 20 s and dried in a moderate air stream to prevent charge leakage during test operation.

Table J.1 – Dimensions of the standard test modules

Type of modules	Diameter (mm)	Thickness (mm)
Small	9,0 ± 0,1	1,3 ± 0,1
Large	25,5 ± 0,2	1,3 ± 0,1

J.3 Test equipment (CDM simulator)

J.3.1 Test equipment design

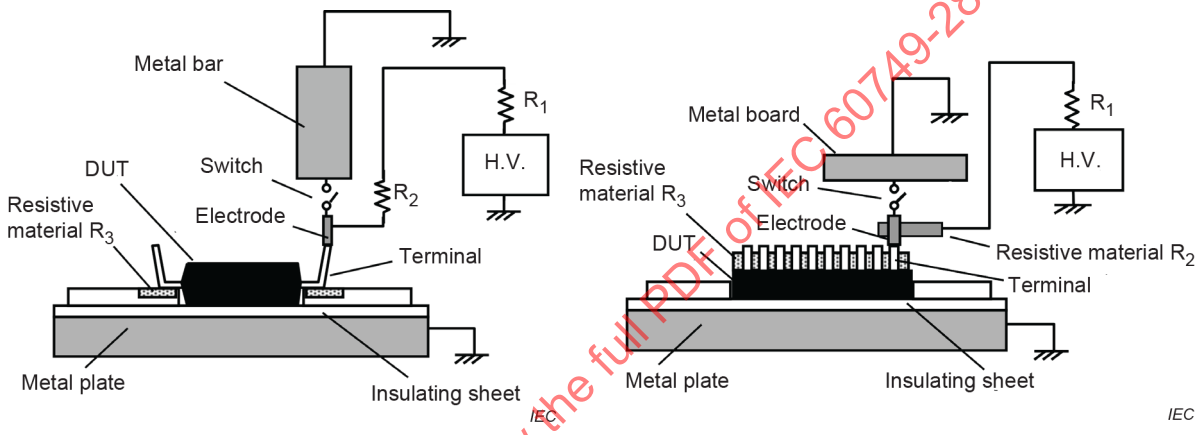
The test equipment should be designed on the basis of the test circuits described below and should satisfy the verification conditions specified in Clause J.4.

J.3.2 DUT (device under test) support

The DUT should be capable of being placed on an insulating sheet attached to a metal plate as shown in Figure J.1. The metal plate should be of sufficiently wide area to contain the DUT and should be able to maintain ground potential. The insulating sheet is 0,4 mm ± 0,04 mm in thickness, relative permittivity 4,0 ± 0,5 at 1 GHz, volume resistivity 1×10^{15} Ωm or more and with a breakdown voltage higher than the test voltage. A glass epoxy material (e.g. FR-4) is in the range of a relative permittivity of 4,0 ± 0,5 at 1 GHz.

J.3.3 Metal bar/board

The metal bar/board is connected to ground potential. The shape of the metal bar/board is a column, a square pillar, a disc or a square board. The metal bar/board is connected to the ground with a wire (connect the wire to the grounding connection on the housing of the test equipment). The test equipment should meet the verification specified in Clause J.4 by changing the size and configuration of the metal bar/board, and the length of the electrode.



a) Example of use of a metal bar

b) Example of use of a metal board and a resistive material R_2

Figure J.1 – Examples of discharge circuit where the discharge is caused by closing the switch

J.3.4 Equipment setup

All of the terminals of the DUT should be capable of maintaining the test potential of the high voltage power supply (H.V.) as shown in Figure J.1. When a high-voltage power supply is to be connected to the terminals of the DUT via a wire, a charging resistor R_1 that is capable of withstanding the test voltage is connected in series between the power supply and the terminals. Resistor R_1 should have a resistance in the range of 10 MΩ to 100 MΩ, but it can be greater provided it meets the conditions prescribed in J.4. When a high-voltage power supply is connected to the terminals of the DUT via an electrode, a resistor/resistive material R_2 with a resistance in the range of 1 MΩ to 10 MΩ is connected in series near the electrode.

The position of R_2 is to be close to the electrode to prevent the wiring being affected during discharges. When R_2 is a resistive material, as shown in Figure J.1 b), connect with the electrode directly.

It is recommended that a resistive material R_3 should be connected to all the terminals of the DUT to ensure that the potentials of all the terminals coincide with the test voltage (see J.5.2 b)). The volume resistivity of the resistive material R_3 should be 1×10^4 Ωm to 1×10^8 Ωm. When the resistive material R_3 cannot make contact with all terminals of the DUT, as a minimum, the test terminal and power pins of the DUT should be capable of being charged (see J.4.3).

J.4 Verification of test equipment

J.4.1 General description of verification test equipment

The verification test measures the discharge current flow to the metal bar/board from the standard test module as shown in Figure J.2.

In practice, for the actual verification, a current sensor, such as the current probe, is added to the equipment. The idealised parameters, without current sensor, are specified in Figure J.3, Table J.2 and Table J.3.

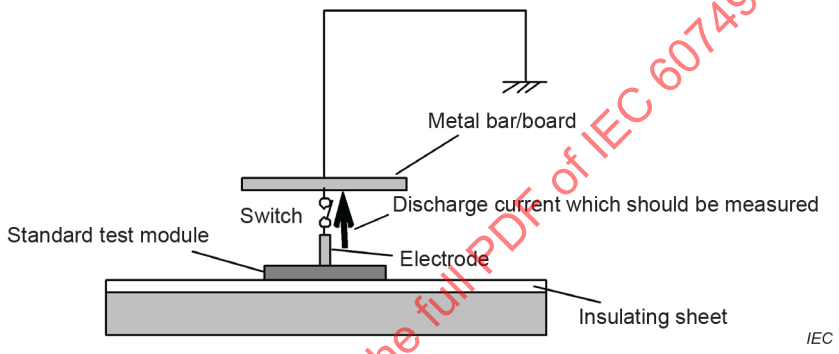


Figure J.2 – Verification test equipment for measuring the discharge current flowing to the metal bar/board from the standard test module

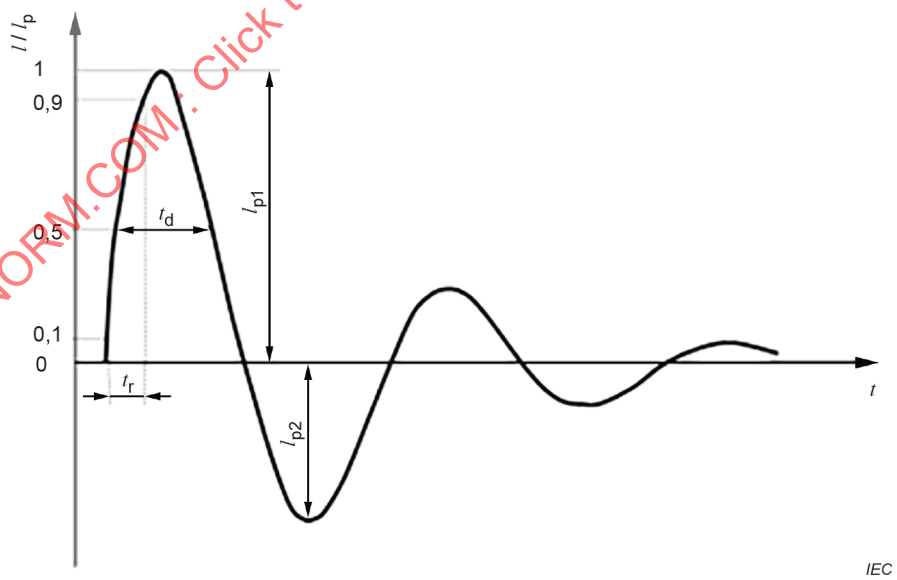


Figure J.3 – Current waveform

Table J.2 – Specified current waveform

Parameter	Unit	Symbol	Specified values	
			Small standard test module	Large standard test module
Rise time	ps	t_r	≤ 350	≤ 450
Pulse width	ps	t_d	325 to 725	500 to 1 000
Peak current	A	I_{p1}	(see Table J.3)	(see Table J.3)
Undershoot current	A	I_{p2}	< 0,7 × I_{p1}	< 0,5 × I_{p1}

Table J.3 – Range of peak current I_{p1} for test equipment

Verification voltage (V)	Values of peak current I_{p1} (A)	
	Small standard test module	Large standard test module
125	1,1 to 1,6	2,1 to 3,1
250	2,2 to 3,1	4,2 to 6,2
500	4,4 to 6,2	8,4 to 12,4
750	6,6 to 9,3	12,6 to 18,6
1 000	8,8 to 12,4	16,8 to 24,8

J.4.2 Instruments for measurement

An oscilloscope with a single shot bandwidth of at least 1 GHz (2 GHz is recommended) with 50 Ω input impedance is used. When a sampling-type oscilloscope is used, a minimum real-time sample rate of 5 GHz is used.

A current probe with bandwidth of at least 2 GHz is used to evaluate the current measurement circuit described in J.4.3, prior to verification of the test equipment.

J.4.3 Verification of test equipment, using a current probe

J.4.3.1 Verification circuit

In order to measure the applied voltage using a current probe, a metal wire of 8 mm in length is added to the standard test module specified in J.2. As shown in Figure J.4, the test equipment is verified by measuring the discharge current from a standard test module to the metal bar/board with the oscilloscope and current probe specified in J.4.2. Since the current probe will not be able to withstand the high voltage required by this method, it will be necessary to maintain the insulation between the current probe and the high-voltage circuit.

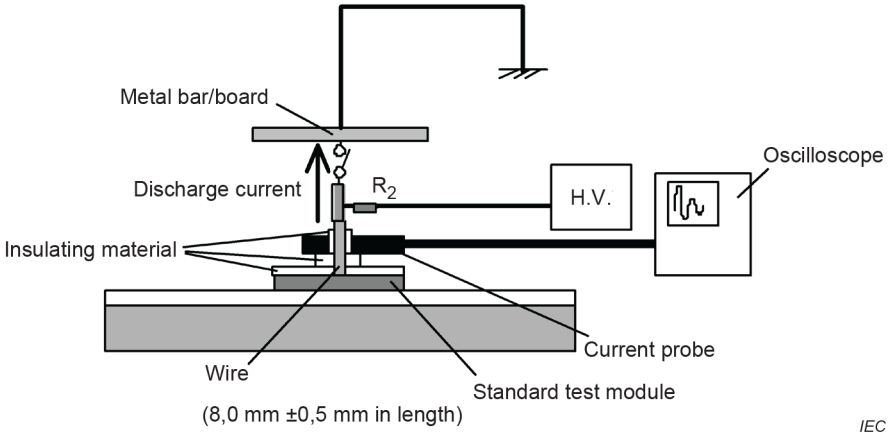


Figure J.4 – Measurement circuit for verification method using a current probe

J.4.3.2 Verification procedure

Verification is carried out as follows.

a) Clean the standard test modules and the insulating sheet using isopropanol.

b) Place the standard test module on the insulating sheet covering the metal plate. After passing a wire 8 mm in length through the hole for measurement of the current probe, the standard test module and the probe of the CDM equipment are connected to both ends of a wire, as shown in Figure J.4.

c) Apply a voltage to the standard test module. Unless otherwise specified, the voltages are +125 V, −125 V, +250 V, −250 V, +500 V, −500 V, +750V, −750V, +1 000 V and −1 000 V to meet the test voltage range. When a test exceeding 1 000 V is performed, a higher voltage such as 2 000 V is additionally applied.

d) The current waveform is measured with the current measurement circuit by closing the switch.

e) The value other than the peak current satisfies Figure J.3 and Figure J.2, and the peak current complies with Table J.4.

NOTE In the measuring method as shown in Figure J.4, the inclusion of an 8 mm wire spacer reduces the resultant peak current to the levels shown in Table J.4. A good correlation has been established using this method between the values in Table J.3 and Table J.4.

Table J.4 – Specification of peak current I_{p1} for the current probe verification method

Verification voltage (V)	Values of peak current I_{p1} (A)	
	Small standard test module	Large standard test module
125	0,9 to 1,3	1,7 to 2,6
250	1,8 to 2,6	3,5 to 5,2
500	3,6 to 5,2	7,0 to 10,3
750	5,4 to 7,8	10,5 to 15,5
1 000	7,3 to 10,4	14,0 to 20,6

J.5 Test procedure

J.5.1 Initial measurement

Complete DC parametric and functional testing are performed in accordance with the applicable device specification at ambient temperature, followed by testing at maximum operating temperature or the temperature required by the relevant specification.

J.5.2 Tests

Testing is performed as follows.

a) Place a DUT on the insulating sheet. The ambient temperature during testing is 25 °C ± 5 °C.

b) Connect all the terminals of the DUT to the resistive material R_3 if required in the relevant specification. Connect the electrode to the test terminal with the switch opened (see Figure J.1).

c) If the DUT has a special isolated structure where the whole DUT is not fully charged from the test terminal, connect all the terminals or all the power supply terminals of the DUT to the resistive material R_3 as shown in Figure J.1.

d) Set the high voltage power supply to the test voltage specified in the relevant specification.

e) Close the switch (see Figure J.1). Confirm the contact between the electrode/front end and the terminal of the DUT during the test.

f) Unless otherwise detailed in the relevant specification, one discharge is performed. When multiple discharges are to be made, repeat the instructions given in steps c) and d). However, there should be an interval of 0,1 s or more between discharges. Reverse the polarity of the testing voltage and perform steps d) to f) if it is detailed in the relevant specification.

g) Perform steps b) to f) for the next test terminal and repeat this procedure to test all the terminals.

h) Reverse the polarity of the testing voltage and perform steps b) to g). When step g) is completed, perform intermediate measurements or perform steps a) to g) on another DUT.

J.5.3 Intermediate and final measurement

Complete DC parametric and functional testing are performed in accordance with the applicable device specification at ambient temperature, followed by testing at maximum operating temperature or the temperature required by the relevant specification.

J.6 Failure criteria

The test is considered to have failed if, after exposure to ESD, the tested component no longer meets its data sheet specifications.

J.7 Classification criteria

All DUT should meet the test requirements of this document up to a particular voltage level in order for the part to be classified as meeting a particular sensitivity classification. Classification levels are shown in Table 3.

J.8 Summary

The following should be detailed in the relevant specification:

a) voltage used for verification (refer to J.4.3.2 c);

b) parameters and conditions of initial measurement (refer to J.5.1);

c) ambient temperature during test (when other than specified) (refer to J.5.2 a));

d) connection of the resistive material R3 to all terminals of DUT if needed (refer to J.5.2 b));

e) test voltage (refer to J.5.2 d));

f) number of samples to be tested (refer to J.5.1 and J.5.3);

g) number of discharges (when other than specified) (refer to J.5.2 f));

h) interval between repeated discharges (when other than specified) (refer to J.5.2 f));

i) procedures for reversing the testing voltage (when other than specified) (refer to J.5.2 f)) and J.5.2 h));

j) parameters and conditions of intermediate and final measurements (when other than specified) (refer to J.5.3).

Bibliography

IEC 60749-26, *Semiconductor devices – Mechanical and climatic test methods – Part 26: Electrostatic discharge (ESD) sensitivity testing – Human body model (HBM)*

SOMMAIRE

COMMISSION ÉLECTROTECHNIQUE INTERNATIONALE

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DISPOSITIFS À SEMICONDUCTEURS – MÉTHODES D'ESSAIS MÉCANIQUES ET CLIMATIQUES –

Partie 28: Essai de sensibilité aux décharges électrostatiques (DES) – Modèle de dispositif chargé (CDM) – niveau du dispositif

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L'IEC 60749-28 a été établie par le comité d'études 47 de l'IEC: Dispositifs à semiconducteurs, en collaboration avec le comité d'études 101 de l'IEC: Électrostatique. Il s'agit d'une Norme internationale.

La présente norme est fondée sur le document ANSI/ESDA/JEDEC JS-002-2018. Elle est utilisée avec l'autorisation des détenteurs des droits d'auteur, ESD Association et JEDEC Solid state Technology Association. Le document ANSI/ESDA/JEDEC JS-002-2018 présente la méthode induite par champ (FI - *field-induced*). Une méthode alternative, la méthode par contact direct (DC - *direct contact*), est décrite à l'Annexe J.

Cette deuxième édition annule et remplace la première édition parue en 2017. Cette édition constitue une révision technique.

Cette édition contient les modifications techniques majeures suivantes par rapport à l'édition précédente:

a) ajout d'un nouveau paragraphe et d'une nouvelle annexe relatifs aux problèmes associés à l'essai de CDM des circuits intégrés et des semiconducteurs discrets dans de très petits boîtiers;

b) introduction de modifications afin de clarifier le nettoyage des dispositifs et des appareils d'essai.

Le texte de cette Norme internationale est issu des documents suivants:

Projet	Rapport de vote
47/2746/FDIS	47/2754/RVD

Le rapport de vote indiqué dans le tableau ci-dessus donne toute information sur le vote ayant abouti à son approbation.

La langue employée pour l'élaboration de cette Norme internationale est l'anglais.

Le présent document a été rédigé selon les Directives ISO/IEC, Partie 2, il a été développé selon les Directives ISO/IEC, Partie 1 et les Directives ISO/IEC, Supplément IEC, disponibles sous www.iec.ch/members_experts/refdocs. Les principaux types de documents développés par l'IEC sont décrits plus en détail sous http://www.iec.ch/standardsdev/publications.

Une liste de toutes les parties de la série IEC 60749, publiées sous le titre général *Dispositifs à semiconducteurs – Méthodes d'essai mécaniques et climatiques* peut être consultée sur le site web de l'IEC.

Le comité a décidé que le contenu du présent document ne sera pas modifié avant la date de stabilité indiquée sur le site web de l'IEC sous "http://webstore.iec.ch" dans les données relatives au document recherché. À cette date, le document sera

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- amendé.

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INTRODUCTION

Les premiers modèles et les premières normes d'essai de décharges électrostatiques (DES) simulaient l'approche d'un dispositif par un objet chargé, ainsi que sa décharge dans ledit dispositif. Le modèle du corps humain (HBM - *human body model*), défini dans l'IEC 60749-26, en constitue l'exemple le plus courant. Toutefois, face à une utilisation accrue de systèmes de manipulation automatisée des dispositifs, un autre mécanisme de décharge potentiellement destructeur, le modèle de dispositif chargé (CDM - *charged device model*), devient de plus en plus important. Dans le modèle CDM, le dispositif proprement dit est chargé (par exemple, par glissement sur une surface (charge triboélectrique) ou par induction de champ électrique) puis déchargé rapidement (par un événement de DES) du fait de son rapprochement avec un objet conducteur. La décharge métal-métal, qui constitue une caractéristique essentielle du CDM, entraîne un transfert de charge très rapide par l'intermédiaire d'un arc de claquage dans l'air. La méthode d'essai de CDM simule également les décharges métal-métal issues d'autres scénarii similaires, comme la décharge d'objets métalliques chargés dans des dispositifs à un potentiel différent.

La quantification et la reproduction exactes de cet événement de décharge métal-métal rapide s'avèrent très difficiles, voire impossibles, en raison des limites de l'appareil de mesure et de son influence sur l'événement de décharge. La décharge de CDM s'effectue généralement en quelques nanosecondes, avec l'observation de courants de crête de dizaines d'ampères. Le courant de crête dans le dispositif varie de manière considérable selon de nombreux facteurs, y compris le type de boîtier et les parasites. Le dommage diélectrique constitue le mécanisme de défaillance type observé dans les dispositifs MOS pour le modèle CDM, bien qu'un autre type de dommage ait toutefois été constaté.

La sensibilité d'un dispositif donné à la tension de charge de CDM dépend du boîtier. Par exemple, le même circuit intégré (IC - *integrated circuit*) dans un petit boîtier peut être moins sensible à un dommage de CDM à une tension donnée par comparaison avec ce même IC dans un plus grand boîtier de même type. Il a été démontré que la sensibilité aux dommages de CDM présente une meilleure corrélation avec les niveaux de courant de crête qu'avec la tension de charge.

DISPOSITIFS À SEMICONDUCTEURS – MÉTHODES D'ESSAIS MÉCANIQUES ET CLIMATIQUES –

Partie 28: Essai de sensibilité aux décharges électrostatiques (DES) – Modèle de dispositif chargé (CDM) – niveau du dispositif

1 Domaine d'application

La présente partie de l'IEC 60749 établit la procédure d'essai, d'évaluation et de classification des dispositifs et des microcircuits selon leur susceptibilité (sensibilité) au dommage ou leur dégradation par suite de leur exposition à une décharge électrostatique (DES) sur un modèle défini de dispositif chargé (CDM) induit par champ. Tous les dispositifs à semiconducteurs, circuits à couches minces, dispositifs à ondes acoustiques de surface (OAS), dispositifs optoélectroniques, circuits intégrés hybrides (HIC - *hybrid integrated circuits*) et modules multipuces (MCM - *multi-chip modules*) en boîtiers qui contiennent l'un de ces dispositifs doivent être évalués selon le présent document. Pour effectuer les essais, les dispositifs sont assemblés dans un boîtier similaire à celui prévu dans l'application finale. Le présent document CDM ne s'applique pas aux appareils d'essai de modèles de décharge avec support. Il décrit en revanche la méthode induite par champ (FI - *field-induced*). Une méthode alternative, la méthode par contact direct (DC - *direct contact*), est décrite à l'Annexe J.

L'objet du présent document est d'établir une méthode d'essai qui reproduit les défaillances du CDM et de fournir des résultats d'essais de DES de CDM fiables et reproductibles d'un appareil d'essai à un autre, indépendamment du type de dispositif. Des données reproductibles permettent des classifications et des comparaisons exactes des niveaux de sensibilité de DES de CDM.

2 Références normatives

Le présent document ne contient aucune référence normative.

3 Termes et définitions

Pour les besoins du présent document, les termes et définitions suivants s'appliquent.

L'ISO et l'IEC tiennent à jour des bases de données terminologiques destinées à être utilisées en normalisation, consultables aux adresses suivantes:

- IEC Electropedia: disponible à l'adresse http://www.electropedia.org/
- ISO Online browsing platform: disponible à l'adresse http://www.iso.org/obp

3.1
DES de CDM
décharge électrostatique de modèle de dispositif chargé
décharge électrostatique (DES) qui utilise le modèle de dispositif chargé (CDM) pour simuler l'événement réel de décharge qui se produit lors de la décharge rapide d'un dispositif chargé dans un autre objet à un potentiel électrostatique inférieur et par l'intermédiaire d'une broche ou d'une borne unique

3.2
appareil d'essai de DES de CDM
appareil d'essai de décharge électrostatique de modèle de dispositif chargé
appareillage qui simule l'événement DES CDM au niveau du dispositif au moyen de la méthode d'essai sans support

Note 1 à l'article: Le terme "appareillage" désigne un "appareil d'essai" dans le présent document.

3.3
C_{Faible}
capacité d'un dispositif placé sur une plaque de champ pour un circuit intégré ou un semiconducteur discret, à laquelle ou au-dessous de laquelle il a été déterminé qu'un essai de CDM n'est pas exigé lorsque les conditions spécifiées sont satisfaites

3.4
couche diélectrique
isolateur à couche mince placé au sommet de la plaque de champ afin de la séparer du dispositif

3.5
plaque de champ
plaque conductrice qui permet d'élever le potentiel du dispositif en essai (DEE) par couplage capacitif

Note 1 à l'article: Voir la Figure 1.

3.6
plan de masse
plaque conductrice qui permet de compléter les circuits de mise à la terre/décharge du DEE

Note 1 à l'article: Voir la Figure 1.

3.7
tension logicielle
tension saisie par l'utilisateur/opérateur qui, lorsqu'elle est combinée au facteur d'échelle ou au décalage, règle la tension réelle de la plaque de champ du système afin d'obtenir les paramètres de la forme d'onde

Note 1 à l'article: Les paramètres de la forme d'onde sont définis dans le Tableau 1 ou le Tableau 2.

3.8
condition d'essai
TC
tension de plaque de l'appareil d'essai qui satisfait aux conditions des paramètres de la forme d'onde

Note 1 à l'article: Les conditions des paramètres de la forme d'onde figurent dans une colonne spécifique du Tableau 1 et du Tableau 2.

Note 2 à l'article: L'abréviation "TC" est dérivée du terme anglais développé correspondant "test condition".

4 Appareillage exigé

4.1 Appareil d'essai de DES de CDM

4.1.1 Généralités

La Figure 1 représente le schéma matériel du montage d'un appareil d'essai de CDM destiné à réaliser un essai de DES de CDM induit par champ avec utilisation par hypothèse d'une sonde de courant résistif. Le DEE peut être un dispositif réel ou l'un des deux modules de vérification (disques métalliques) décrits à l'Annexe A. La broche pogo doit être connectée au plan de

masse avec un chemin de courant de 1 Ω et une largeur de bande minimale (BW - *bandwidth*) de 9 gigahertz (GHz). La connexion broche pogo de 1 Ω / terre du détecteur de courant résistif peut prendre la forme d'une combinaison parallèle d'une résistance de 1 Ω entre la broche pogo et le plan de masse, et de l'impédance de 50 Ω de l'oscilloscope et son câble coaxial. À la Figure 1, K1 représente le commutateur entre la charge de la plaque de champ et sa mise à la terre. Les appareils d'essai de DES de CDM utilisés dans le contexte du présent document doivent satisfaire aux caractéristiques de la forme d'onde spécifiées à la Figure 2, ainsi que dans le Tableau 1 et le Tableau 2, sans la présence de dispositifs passifs ou actifs supplémentaires, tels que des ferrites, dans l'ensemble capteur.

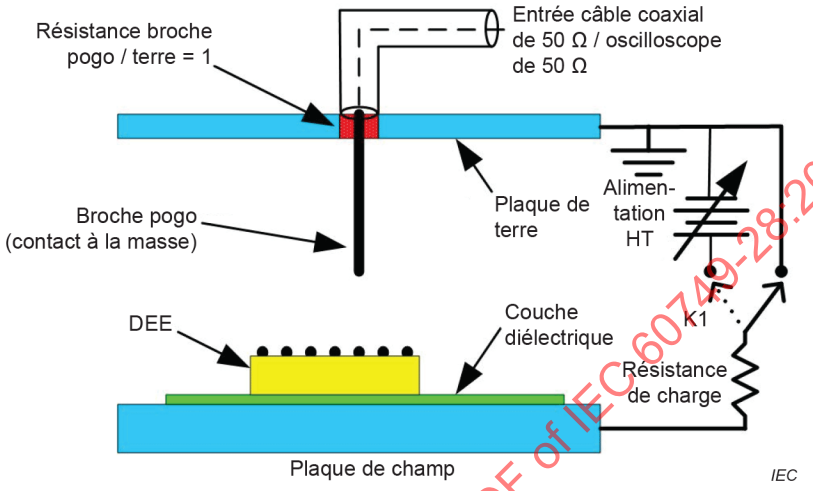

Figure 1 – Schéma matériel simplifié de l'appareil d'essai de CDM

Lors de la constitution de l'appareillage d'essai, il convient de réduire le plus possible les parasites des chemins de charge et de décharge dans la mesure où les parasites d'inductance-capacité de la résistance (RLC - *resistance inductance-capacitance*) dudit appareillage influent de manière significative sur les résultats d'essai.

Dans le cas de l'appareillage existant, il est recommandé de contacter le personnel d'entretien qualifié afin de déterminer la conformité au présent document lors de l'élimination des composants de ferrite.

4.1.2 Détecteur de courant

Un détecteur de courant doit être intégré au plan de masse. La résistance de ce détecteur doit avoir une valeur de (1,0 ± 10 %) Ω. Une résistance, telle qu'elle est spécifiée en 4.1.1, doit être utilisée comme détecteur de courant. La valeur de la résistance (y compris la terminaison câble/oscilloscope de 50 Ω) doit être mesurée au moyen d'un ohmmètre tel qu'il est décrit en 4.5. Cette valeur doit permettre de calculer le premier courant de crête.

Le détecteur de courant doit avoir une réponse en fréquence minimale de 9 GHz (spécifiée par un affaiblissement maximal de 3 dB à 9 GHz).

4.1.3 Plan de masse

L'ensemble capteur doit contenir un plan de masse carré avec la broche de sonde disposée en son centre comme cela est représenté à la Figure 1. Les dimensions du plan de masse doivent être de 63,5 mm × 63,5 mm ± 6,35 mm (2,5 pouces × 2,5 pouces ± 0,25 pouce).

4.1.4 Plaque de champ /couche diélectrique de la plaque de champ

La planéité de surface de la plaque de champ ne doit pas varier de plus de ± 0,127 mm (0,005 pouce). Il convient que la couche diélectrique de la plaque de champ soit constituée d'un matériau FR4 ou d'un matériau en verre-époxy analogue. Dans le cas du matériau FR4, il

convient que l'épaisseur et la tolérance d'épaisseur de cette couche diélectrique soient de 0,381 mm ± 0,0254 mm (0,015 pouce ± 0,001 pouce) afin d'obtenir une plage de mesure de la capacité (comme cela est spécifié à l'Annexe B normative) définie dans le Tableau A.1.

Lors de l'utilisation d'un matériau différent, le choix de son épaisseur est déterminé par l'obtention d'une plage de mesure de la capacité telle qu'elle est définie dans le Tableau A.1.

4.1.5 Résistance de charge

La résistance de charge nominale représentée à la Figure 1 doit être supérieure ou égale à 100 MΩ.

Des valeurs de résistance supérieures à 100 MΩ peuvent être utilisées. Cette possibilité peut toutefois ne pas permettre une charge complète de dispositifs de très grande taille (se reporter à 5.9 et à l'Annexe I) préalablement à leur décharge par l'ensemble capteur. L'ajout d'un délai entre les décharges dans le logiciel de programmation de l'appareil d'essai de CDM permet de surmonter cet effet. Lors de l'utilisation d'une résistance supérieure à 100 MΩ, il est recommandé de caractériser l'appareil d'essai ou le dispositif proprement dit de manière à déterminer si la décharge de dispositifs de grande taille nécessite un délai. Une procédure de cette caractérisation de délai pour les dispositifs de grande taille est indiquée à l'Annexe I.

4.2 Appareil de mesure de la forme d'onde

4.2.1 Généralités

L'appareil de mesure de la forme d'onde CDM doit être constitué des composants suivants.

4.2.2 Ensembles de câbles

Ensembles de câbles avec une perte totale combinée du câble interne de l'appareil d'essai et de son câble externe inférieure ou égale à 2 dB à des fréquences jusqu'à 5 GHz inclus et une impédance nominale de 50 Ω.

4.2.3 Appareil pour le mesurage d'une forme d'onde à largeur de bande élevée

4.2.3.1 Oscilloscope à largeur de bande élevée

Oscilloscope ou numériseur de transitoires avec une largeur de bande minimale en temps réel (impulsion unique) de 3 dB à une fréquence d'au moins 6 GHz, ainsi qu'une fréquence d'échantillonnage ≥ 20 gigaéchantillon/s et une impédance d'entrée nominale de 50 Ω.

4.2.3.2 Affaiblisseur

Un affaiblisseur de 20 dB avec une précision de ±0,5 dB, une largeur de bande avec une fréquence d'au moins 12 GHz et une impédance de 50 Ω ± 5,0 Ω.

4.2.4 Appareil pour le mesurage d'une forme d'onde de 1,0 GHz

4.2.4.1 Oscilloscope à 1 GHz

Oscilloscope ou numériseur de transitoires avec une largeur de bande en temps réel (impulsion unique) de 3 dB à une fréquence de 1 GHz, et une impédance d'entrée nominale de 50 Ω. La fréquence d'échantillonnage doit être ≥ 5 gigaéchantillon/s.

NOTE L'utilisateur a la possibilité de recourir à un oscilloscope à largeur de bande plus élevée, ainsi qu'à un filtre matériel ou logiciel afin de produire une largeur de bande et une fréquence d'échantillonnage équivalentes à celles spécifiées en 4.2.4.1.

4.2.4.2 Affaiblisseur

Un affaiblisseur de 20 dB avec une précision de ± 0,5 dB, une largeur de bande avec une fréquence d'au moins 4 GHz et une impédance de 50 Ω ± 5 Ω.

4.3 Modules de vérification (disques métalliques)

Le grand module de vérification doit avoir une capacité de (55 ± 5 %) pF, tandis que le petit module de vérification doit avoir une capacité de (6,8 ± 5 %) pF. Se reporter à l'Annexe A normative pour les informations concernant les dimensions physiques des modules de vérification, et à l'Annexe B normative pour les informations concernant la procédure de mesure de la capacité.

4.4 Capacimètre

Le capacimètre avec une résolution de 0,2 pF, une exactitude de mesure de 3 %, et une fréquence de mesure de 1,0 MHz comme cela est décrit à l'Annexe B normative.

4.5 Ohmmètre

L'ohmmètre utilisé pour mesurer la résistance de la sonde résistive doit être capable d'effectuer des mesurages avec une exactitude de 0,01 Ω. L'utilisation de connexions à 4 fils de Kelvin est recommandée.

5 Exigences de qualification périodique de l'appareil d'essai et exigences concernant les enregistrements et la vérification de la ou des formes d'onde

5.1 Présentation des évaluations exigées de l'appareil d'essai de CDM

L'appareil d'essai de CDM doit faire l'objet d'une qualification, d'une requalification et d'une vérification périodique comme cela est décrit en 5.5 et 5.6.

NOTE 1 Les couches diélectriques, plans de masse (plaques de terre), la résistance (sonde) de décharge coaxiale, la distance entre le plan de masse et la plaque de champ, les modules de vérification et les contacts de décharge (par exemple, broches pogo) constituent des éléments essentiels de la constitution de l'appareil d'essai. Toute modification de ces éléments exige une vérification de la forme d'onde.

NOTE 2 Des modifications de la forme de l'impulsion de décharge, même si elles peuvent toujours relever d'une spécification, peuvent indiquer une détérioration du chemin de décharge.

5.2 Matériel de capture de la ou des formes d'onde

La capture de la ou des formes d'onde exige les instruments suivants, ainsi que la procédure suivante de détermination de la tension de consigne de l'appareil d'essai:

- un oscilloscope tel qu'il est spécifié en 4.2;
- un affaiblisseur et un ensemble de câbles tels qu'ils sont définis en 4.2;
- des modules de vérification (tels qu'ils sont décrits en 4.3) avec les dimensions et attributs énumérés à l'Annexe A normative et la méthode de mesure énumérée à l'Annexe B normative.

5.3 Configuration de capture de la ou des formes d'onde

La configuration de capture de la ou des formes d'onde doit suivre les étapes suivantes :

a) nettoyer les modules de vérification. Éviter tout contact cutané avec les modules avant et pendant les essais. Une procédure recommandée est décrite à l'Annexe A normative;

b) nettoyer à l'aide d'un tampon à l'alcool la sonde de décharge et la plaque de charge de champ sur laquelle est placé le dispositif afin d'éliminer toute contamination de surface

susceptible d'entraîner une perte de charge. Vérifier que la broche pogo est exempte de matières particulaires;

c) fixer l'affaiblisseur de 20 dB approprié sur l'oscilloscope tel qu'il est décrit en 4.2.3.2. Fixer une extrémité de l'ensemble de câbles externes sur l'affaiblisseur, comme cela est décrit en 4.2.2, et fixer l'autre extrémité dudit ensemble à l'appareil d'essai de CDM. Vérifier l'étanchéité de toutes les liaisons de la chaîne de mesure.

Voir l'Annexe F informative pour un exemple de réglages de l'oscilloscope et de capture de formes d'onde.

5.4 Procédure de capture de la ou des formes d'onde

La procédure de capture de la ou des formes d'onde doit être exécutée comme suit:

a) placer le module de vérification à utiliser sur la couche diélectrique de la plaque de champ, avec l'assurance d'un contact étroit entre ladite couche et le module de vérification;

b) régler le potentiel de la plaque de champ sur la tension nécessaire pour la condition d'essai exécutée;

c) aligner le contact à la masse sur approximativement le centre du module de vérification;

d) la méthode de décharge simple ou la méthode de double décharge telle qu'elle est décrite à l'Article G.2 ou à l'Article G.3 respectivement, peut être utilisée, mais il convient toutefois que la méthode de décharge choisie soit conforme au mode d'essai des produits. Lorsque la méthode de double décharge est appliquée, les formes d'onde pour des impulsions positives et des impulsions négatives exigent une modification des conditions de déclenchement de l'oscilloscope afin de capturer uniquement des impulsions positives ou négatives;

e) décharger au moins dix fois le module de vérification à la polarité vérifiée;

f) observer au moins dix formes d'onde successives pendant la série de décharges ci-dessus et enregistrer les paramètres moyens de formes d'onde pour I_p, T_r, largeur à mi-crête (FWHM), et Ip2 pour ce groupe de formes d'onde comme cela est représenté à la Figure 2;

g) lorsque les caractéristiques de formes d'onde ne satisfont pas aux exigences telles qu'elles sont définies dans le Tableau 1 ou le Tableau 2 pour la condition d'essai cible (voir 5.6 et 5.7 pour le tableau et les conditions d'essai à appliquer), nettoyer une nouvelle fois les modules de vérification et le contact à la masse, contrôler l'étanchéité de toutes les liaisons, effectuer des ajustements de la tension de la plaque de champ et répéter les étapes a) à g).

Lorsque cette procédure ne fonctionne toujours pas, contrôler le vide du système ou envisager le remplacement du contact à la masse. Consulter le fabricant de l'appareil d'essai pour de plus amples informations.

Répéter la procédure pour la polarité opposée.

5.5 Procédure de qualification/requalification de l'appareil d'essai de CDM

5.5.1 Procédure de qualification/requalification de l'appareil d'essai de CDM

La procédure de qualification/requalification a pour objet de déterminer la tension de plaque de champ nécessaire pour chaque réglage de condition d'essai (125 – 1 000) dans le Tableau 3 afin de produire un courant de crête dans les plages qui correspondent au Tableau 2, et par conséquent qui correspondent aux niveaux de classification tels qu'ils sont spécifiés dans le Tableau 3.

Deux procédures alternatives de mode de qualification et de contrôle de routine du système d'essai de CDM sont présentées à l'Annexe H. Ces procédures sont fondées sur des systèmes d'essai de CDM généralement disponibles et proposent deux méthodes d'ajustement de la tension de plaque de champ afin de satisfaire aux paramètres des formes d'onde spécifiés dans le Tableau 2.

Les fabricants de systèmes d'essai de CDM, ou les opérateurs de tels systèmes d'essai peuvent élaborer d'autres procédures de qualification à partir des deux procédures présentées à l'Annexe H, tant que ces procédures produisent des formes d'onde qui satisfont aux exigences définies dans le Tableau 2 pour les différentes conditions d'essai.

Il est recommandé que les réglages déterminés à partir de cette procédure de qualification soient enregistrés pour un système d'essai particulier, ainsi qu'une largeur de bande d'oscilloscope et une polarité tout aussi particulières. Cette procédure permet de détecter une dérive du système dans la durée, ce qui peut indiquer un problème plus important avec le système. Voir l'Article H.3 pour des exemples.

Exécuter les étapes de configuration et de capture des formes d'onde comme cela est décrit en 5.3 et 5.5 dans les conditions d'essai 125 – 1 000 définies dans le Tableau 2 pour les deux polarités (positive et négative) au moyen de petits et de grands modules de vérification, et par des mesurages avec l'oscilloscope à largeur de bande élevée comme cela est spécifié en 4.2.3.1. Se reporter à l'Annexe H pour des exemples d'organigrammes des procédures.

Lorsque les plages de tension d'essai sur site local sont toujours plus étroites que la plage ci-dessus (par exemple, conditions d'essai 125 – 500), la réalisation de la qualification dans cette plage plus étroite est admissible.

5.5.2 Conditions qui exigent la qualification/requalification de l'appareil d'essai de CDM

Les situations suivantes exigent la qualification et la requalification de l'appareil d'essai de CDM comme cela est décrit en 5.5:

- essais de réception lors de la livraison de l'appareil d'essai de CDM, généralement réalisé par le fabricant lors de l'installation;
- requalification périodique conformément aux recommandations du fabricant; la durée maximale entre les essais de requalification est de un an;
- après une opération d'entretien ou de réparation susceptible d'altérer la forme d'onde.

5.5.3 Corrélation entre l'oscilloscope à 1 GHz et l'oscilloscope à largeur de bande élevée

Pendant le premier essai de réception, le fabricant de l'appareil d'essai doit utiliser un oscilloscope à largeur de bande élevée comme cela est spécifié en 4.2.3.1 pour la capture initiale des formes d'onde. Lorsque le site d'essai comporte uniquement un oscilloscope à 1 GHz comme cela est spécifié en 4.2.4.1, le fabricant et l'utilisateur final de l'appareil d'essai doivent confirmer leur utilisation de techniques appropriées de filtrage de largeurs de bande, ainsi que la comparaison avec l'oscilloscope fourni par le fabricant de l'appareil d'essai selon laquelle l'oscilloscope de l'utilisateur mesure les formes d'onde de l'appareil d'essai comme cela est défini dans le Tableau 1 pour la validation trimestrielle et de routine des formes d'onde.

NOTE L'option de filtrage logiciel Bessel-Thomson disponible sur de nombreux oscilloscopes prend la forme d'un filtre approprié pour les formes d'onde à largeur de bande élevée, car il s'adapte bien aux données réelles de l'oscilloscope à 1 GHz.

La vérification de la corrélation des oscilloscopes doit être répétée lorsque le site d'essai modifie les oscilloscopes à 1 GHz.

5.6 Procédure de vérification trimestrielle et de routine des formes d'onde propre à l'appareil d'essai de CDM

5.6.1 Procédure de vérification trimestrielle des formes d'onde

Exécuter les étapes de configuration et de capture des formes d'onde comme cela est décrit en 5.3 et 5.5 dans les conditions d'essai 125 – 1 000 définies dans le Tableau 1 au moyen de l'oscilloscope à 1 GHz comme cela est spécifié en 4.2.4.1 ou dans les conditions d'essai

définies dans le Tableau 2 au moyen de l'oscilloscope à largeur de bande élevée comme cela est spécifié en 4.2.3.1. Les deux modules de vérification doivent être contrôlés aux polarités positive et négative. Il est recommandé d'utiliser l'oscilloscope à largeur de bande élevée lorsque cette possibilité existe. Se reporter à l'Annexe H pour des exemples d'organigrammes des procédures.

Lorsque les plages de tension d'essai sur site local sont toujours plus étroites que la plage ci-dessus (par exemple, conditions d'essai 125 – 500), la réalisation de la qualification dans cette plage plus étroite est admissible.

Les formes d'onde produites par l'appareil d'essai doivent être soumises à une vérification au moins trimestrielle.

5.6.2 Procédure de vérification de routine des formes d'onde

5.6.2.1 Généralités

Exécuter les étapes de configuration et de capture des formes d'onde comme cela est décrit en 5.3 et 5.5 dans la condition 500 définie dans le Tableau 1 (oscilloscope à 1 GHz) ou dans le Tableau 2 (oscilloscope à largeur de bande élevée) pour les deux polarités (positive et négative) au moyen du module de vérification qui correspond le mieux à la taille du boîtier soumis à l'essai. Se reporter à l'Annexe H pour des exemples d'organigrammes des procédures.

5.6.2.2 Fréquence de vérification de routine

Initialement, lors de la qualification ou de la requalification de l'appareil d'essai, il convient d'effectuer la vérification de routine des formes d'onde au moins une fois par changement. Lorsque l'essai de contrainte de CDM est effectué par changements consécutifs, les contrôles de forme d'onde à la fin d'un changement peuvent également servir de contrôle initial pour le changement suivant.

Des périodes plus longues entre les contrôles de routine de formes d'onde peuvent être utilisées lorsqu'aucune variation des formes d'onde n'est observée sur plusieurs contrôles consécutifs. La fréquence et la méthode d'essai choisies doivent être documentées. Lorsque, à tout moment, les formes d'onde ne satisfont plus aux limites spécifiées, toutes les données d'essai de contrainte de DES recueillies après le contrôle de forme d'onde satisfaisant précédent doivent être marquées comme non valables et ne doivent pas être utilisées pour la classification.

5.7 Caractéristiques des formes d'onde

Les formes d'onde doivent apparaître comme cela est représenté à la Figure 2 tant pour la polarité positive que pour sa polarité inverse, la polarité négative. Les paramètres moyens de formes d'onde (y compris I_p) tels qu'ils sont réunis par la méthode spécifiée en 5.4 doivent satisfaire aux spécifications du Tableau 1 pour un oscilloscope à 1 GHz et à celles du Tableau 2 pour un oscilloscope à largeur de bande élevée. Lorsqu'un oscilloscope à largeur de bande élevée est utilisé à des fins de qualification et de vérifications trimestrielles et de routine des formes d'onde, il n'est pas nécessaire de prendre en considération les exigences de fréquence de 1 GHz.

Tableau 1 – Caractéristiques des formes d'onde de CDM pour un oscilloscope à largeur de bande de 1 GHz

Oscilloscope à largeur de bande de 1 GHz		**Condition d'essai**									
		TC 125		TC 250		TC 500		TC 750		TC 1 000	
Module de vérification	Sym.	Petit	Grand	Petit	Grand	Petit	Grand	Petit	Grand	Petit	Grand
Courant de crête (A)	I_p	1,0 à 1,6	1,9 à 3,2	2,1 à 3,1	4,2 à 6,3	4,4 à 5,9	9,1 à 12,3	6,6 à 8,9	13,7 à 18,5	8,8 à 11,9	18,3 à 24,7
Temps de montée (ps)	t_r	< 350	< 450	< 350	< 450	< 350	< 450	< 350	< 450	< 350	< 450
Largeur à mi-crête (ps)	FWHM	325 à 725	500 à 1 000	325 à 725	500 à 1 000	325 à 725	500 à 1 000	325 à 725	500 à 1 000	325 à 725	500 à 1 000
Sous-dépassement (A, second pic au maximum)	I_{p2}	<70 % I_p	<50 % I_p	<70 % I_p	<50 % I_p	<70 % I_p	<50 % I_p	<70 % I_p	<50 % I_p	<70 % I_p	<50 % I_p

Tableau 2 – Caractéristiques des formes d'onde de CDM pour un oscilloscope à largeur de bande élevée (≥ 6 GHz)

Oscilloscope à largeur de bande ≥ 6 GHz		**Condition d'essai**									
		TC 125		TC 250		TC 500		TC 750		TC 1 000	
Module de vérification	Sym.	Petit	Grand	Petit	Grand	Petit	Grand	Petit	Grand	Petit	Grand
Courant de crête (A)	I_p	1,4 à 2,3	2,3 à 3,8	2,9 à 4,3	4,8 à 7,3	6,1 à 8,3	10,3 à 13,9	9,2 à 12,4	15,5 à 20,9	12,2 à 16,5	20,6 à 27,9
Temps de montée (ps)	t_r	< 250	< 350	< 250	< 350	< 250	< 350	< 250	< 350	< 250	< 350
Largeur à mi-crête (ps)	FWHM	250 à 600	450 à 900	250 à 600	450 à 900	250 à 600	450 à 900	250 à 600	450 à 900	250 à 600	450 à 900
Sous-dépassement (A, second pic au maximum)	I_{p2}	<70 % I_p	<50 % I_p	<70 % I_p	<50 % I_p	<70 % I_p	<50 % I_p	<70 % I_p	<50 % I_p	<70 % I_p	<50 % I_p

NOTE Les tensions des conditions d'essai 125 à 1 000 qui produisent les plages spécifiées de courant de crête sont ajustées sur la base des tensions d'essai de classification précédentes de 125 V, 250 V, 500 V, 750 V et 1 000 V respectivement. L'Annexe D décrit cette relation entre ce type de tensions et les tensions réglées par l'appareil d'essai exempt de tensions sans ferrite. Les tensions de plaque de champ ajustées par l'appareil d'essai pour obtenir les plages de courant applicables à la plateforme d'appareils d'essai exempts de ferrites définie dans le présent document peuvent varier quelque peu entre les appareils d'essai. L'Annexe H décrit deux méthodes d'ajustement de tension.

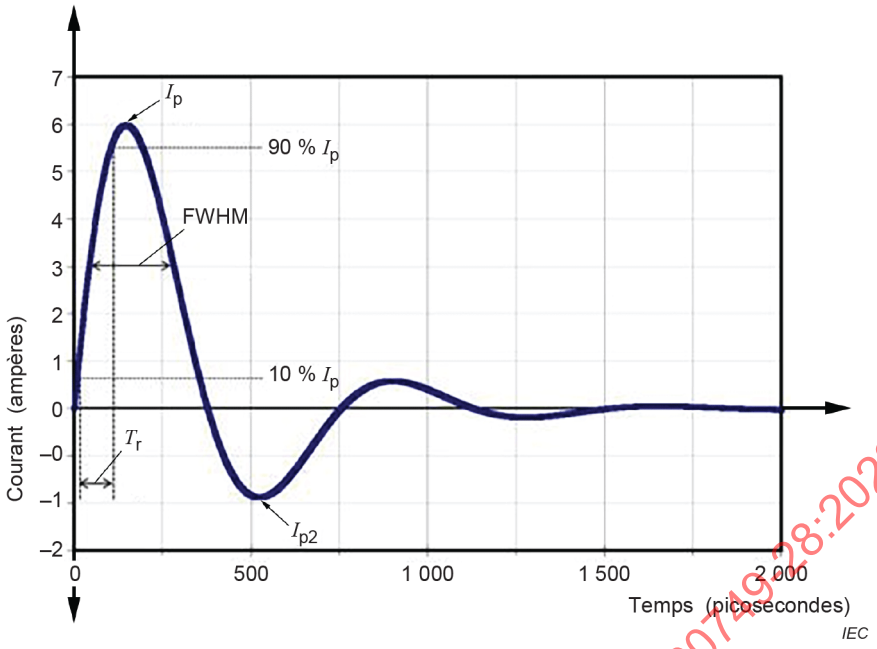

Figure 2 – Forme d'onde et paramètres caractéristiques du CDM

5.8 Documentation

Conserver les enregistrements de formes d'onde pour la qualification de l'appareil d'essai selon la politique interne de l'entreprise. Pour la requalification de l'appareil d'essai, ainsi que pour les vérifications trimestrielle et de routine des formes d'onde, conserver les enregistrements jusqu'à la collecte du prochain ensemble de formes d'onde, ou selon la politique interne de l'entreprise.

5.9 Procédure d'évaluation de la charge complète de l'appareil d'essai d'un dispositif

5.9.1 Comme cela est défini en 4.1.5, il convient que la résistance de charge nominale soit supérieure ou égale à 100 MΩ. En cas de résistance trop importante, un délai de charge supplémentaire peut s'avérer nécessaire pour assurer la charge complète du dispositif. Pour déterminer la nécessité éventuelle d'un délai supplémentaire, suivre la procédure en 5.9.2.

5.9.2 Suivre la procédure ci-dessous avec le grand module de vérification.

a) Régler la tension de plaque de champ à + 250 V (toute tension peut être utilisée, car l'objectif est de contrôler I_p).

b) Les délais de précharge et de postcharge étant tous deux réglés sur 0 ms, collecter 10 formes d'onde et enregistrer la valeur I_p de chacune d'entre elles. Calculer la valeur I_p moyenne des formes d'onde.

c) Le délai de précharge étant réglé sur 500 ms (le délai de postcharge restant réglé sur 0 ms), collecter dix formes d'onde et enregistrer la valeur I_p de chacune d'entre elles. Calculer la valeur I_p moyenne des formes d'onde.

d) Comparer la valeur I_p moyenne du délai de charge de 0 ms et du délai de charge de 500 ms. Lorsque la valeur I_p moyenne est identique pour les deux mesurages, alors un dispositif de même capacité ou de capacité inférieure à celle du grand module de vérification reçoit une charge complète. Lorsque les valeurs I_p moyennes avec un délai de charge de 0 ms et un délai de charge de 500 ms ne correspondent pas, se reporter à l'Annexe I informative pour une procédure de détermination du délai approprié de charge par défaut à ajouter au système.

e) Même en cas de correspondance des deux valeurs I_p moyennes ci-dessus, les dispositifs de très grande taille en boîtier (capacité plus élevée que celle du grand module de vérification) peuvent toujours exiger un délai afin de recevoir une charge complète. Du fait de la grande diversité des techniques de constitution en boîtier des dispositifs, il n'existe aucune dimension exacte quant au mode selon lequel un boîtier particulier I_p peut être comparé au grand module de vérification I_p pour l'évaluation décrite ci-dessus.

f) Pour déterminer si un très grand dispositif en boîtier peut toujours exiger un délai de charge, les étapes a) à d) ci-dessus peuvent être répétées à l'aide du contact à la masse d'un dispositif. Lorsque les valeurs I_p moyennes avec un délai de charge de 0 ms et un délai de charge de 500 ms ne correspondent pas, se reporter à l'Annexe I informative pour une procédure de détermination du délai de charge approprié.

De plus, lorsque les appareils d'essai de CDM comportent des pièces mobiles, il convient que le personnel veille à éviter tout contact avec ces dernières en fonctionnement.

6 Exigences et procédures d'essai de DES de CDM

6.1 Préparation de l'appareil d'essai et des dispositifs

Les dispositifs utilisés pour les essais de contrainte de CDM ne doivent avoir été utilisés pour aucun essai identique antérieur.

Des procédures de prévention des dommages dus aux DES doivent être appliquées avant, pendant et après les essais de CDM et post-paramétriques.

Les dispositifs doivent être propres avant les essais. Au besoin, il convient d'effectuer un nettoyage conformément aux procédures agréées par l'entreprise.

NOTE De l'isopropanol (alcool isopropylique) est généralement utilisé pour le nettoyage.

La sonde et la plaque de champ / couche diélectrique de l'appareil d'essai de CDM doivent être propres et sèches avant les essais. Un nettoyage peut être effectué de manière périodique ou sur la base de la réception des formes d'onde en utilisant de l'isopropanol (alcool isopropylique) avec un pourcentage minimal de 70 %.

6.2 Exigences d'essai

6.2.1 Température et humidité d'essai

L'essai doit être effectué à température ambiante. Il convient que l'humidité au niveau de la tête d'essai ne dépasse pas 30 % HR. Le chauffage ou le refroidissement du dispositif pendant l'essai de CDM n'est pas prévu.

Il convient de placer l'appareil d'essai dans un environnement à température ambiante.

NOTE La répétabilité des formes d'onde dépend fortement de la teneur en humidité de l'air et une humidité relative faible génère une forme d'onde plus stable.

6.2.2 Essai des dispositifs

6.2.2.1 Essai de précontrainte

Préalablement à l'essai de contrainte de DES, des essais statiques et dynamiques complets doivent être réalisés sur tous les dispositifs soumis aux essais. Les résultats des essais paramétriques et fonctionnels doivent se situer dans les limites spécifiées dans les paramètres de la fiche technique.

6.2.2.2 Critères de défaillance

Après l'essai de contrainte de DES, des essais statiques et dynamiques complets doivent être réalisés sur tous les dispositifs soumis à une contrainte. Un dispositif est considéré comme n'ayant pas satisfait aux essais lorsque les résultats des essais paramétriques et fonctionnels ne se situent pas dans les limites spécifiées dans les paramètres de la fiche technique. Une défaillance peut être omise lorsqu'une analyse des défaillances démontre qu'elle n'est pas liée aux DES de CDM.

NOTE 1 Une variation de fuite statique (par exemple, fuite des broches, courant de repos) n'est pas un critère approprié pour déterminer les critères de réussite/échec. Elle peut servir d'indicateur de l'apparition d'un dommage.

NOTE 2 Lorsque l'essai doit être réalisé à des températures différentes, réaliser tout d'abord l'essai à la température la plus basse, puis augmenter la température de manière séquentielle (par exemple, −40 °C, +25 °C, +85 °C).

6.3 Modes opératoires

Les modes opératoires sont les suivants:

a) sauf spécification contraire, obtenir trois échantillons au moins, dont leur satisfaction aux spécifications de données a été vérifiée;

b) il convient que l'essai de CDM commence au niveau le plus faible défini dans le Tableau 3. Il peut néanmoins commencer à tout niveau. Toutefois, lorsque le niveau de tension initiale est supérieur au niveau le plus faible défini dans le Tableau 3 et lorsque le dispositif ne satisfait pas à l'essai à la tension initiale, l'essai doit être recommencé avec trois nouveaux dispositifs au niveau inférieur suivant;

c) pour chaque dispositif, appliquer au moins une décharge positive et une décharge négative à chaque broche. Prévoir un temps suffisant (comme cela est spécifié en 5.9) entre les décharges pour que le dispositif atteigne le niveau maximal de tension d'essai. Les contraintes peuvent être réparties par polarité, avec une taille de l'échantillon d'au moins trois unités par polarité. Les broches peuvent également être réparties en un ou plusieurs ensembles d'échantillons, sous réserve que chaque broche du dispositif soit un membre d'au moins un ensemble. Chaque ensemble doit comporter trois unités au moins.

La méthode de charge induite par champ comporte deux procédures possibles de charge et de décharge du dispositif: procédure unique et double procédure. Les deux procédures produisent des résultats équivalents. Ces procédures sont décrites à l'Annexe G informative.

6.4 Lignes directrices d'enregistrement / consignation dans un rapport de l'essai de CDM

6.4.1 Enregistrement de l'essai de CDM

La procédure d'essai de CDM pour un produit particulier doit être enregistrée et archivée selon la procédure de conservation des données de chaque entreprise. Il convient de fournir sur demande les informations concernant les paramètres de forme d'onde de l'appareil d'essai. Se reporter à l'Article H.3 pour de plus amples informations sur l'enregistrement des paramètres de forme d'onde.

6.4.2 Lignes directrices relatives à la consignation dans un rapport de l'essai de CDM

Les résultats d'essai de CDM des produits (y compris les informations sur les boîtiers) doivent être consignés et doivent figurer dans le rapport de fiabilité des produits.

Afin d'assurer la mise à disposition d'informations sur la manipulation en toute sécurité pour le contrôle de fabrication dans une zone protégée contre les DES, il est vivement recommandé que les fiches techniques des produits disponibles consignent les classifications de CDM.

6.5 Essai des dispositifs dans de petits boîtiers

Il est très difficile de soumettre à l'essai de CDM les circuits intégrés et les semiconducteurs discrets (ICDS - *Integrated circuits and discrete semiconductors*) dans de très petits boîtiers, qui par ailleurs ne satisfont pas à cet essai que rarement en raison de leur faible capacité. Il n'est pas possible de spécifier une dimension de boîtier au-dessous de laquelle un essai de CDM n'est pas nécessaire dans la mesure où différentes techniques et stratégies de protection, ainsi que différents styles de conception présentent des sensibilités différentes aux événements de charge des dispositifs. En l'absence d'autres informations, tous les ICDS doivent être soumis à l'essai. Toutefois, l'Annexe C définit une procédure facultative d'établissement d'une capacité C_{Faible} de circuit intégré pour une technique et un débit de conception spécifiques. Pour les dispositifs avec une capacité inférieure à C_{Faible}, un essai de CDM n'est plus exigé. Il faut partir du principe que les ICDS avec une capacité inférieure à C_{Faible} et qui satisfont aux exigences de l'Annexe C ont un niveau de satisfaction à l'essai de CDM de TC 750 (Niveau de classification C2b dans le Tableau 3).

7 Critères de classification de CDM

Les dispositifs sensibles aux DES (ESDS - *ESD sensitive*) sont classés selon le mode opératoire décrit dans le présent document. Les résultats d'essai de CDM sont spécifiques au type de boîtier particulier utilisé. La classification des dispositifs correspond au niveau le plus élevé de tension de contrainte de DES (polarité positive et polarité négative) auquel un échantillon d'au moins trois dispositifs a satisfait aux essais statiques et dynamiques complets selon les paramètres des fiches techniques après l'essai de DES. Les niveaux de classification des dispositifs de DES de CDM sont présentés dans le Tableau 3.

Tableau 3 – Niveaux de classification des dispositifs de DES de CDM

Niveau de classification [a]	Condition d'essai de classification (en volts) [b]
C0a	< 125
C0b	125 à < 250
C1	250 à < 500
C2a	500 à < 750
C2b	750 à < 1 000
C3	≥ 1 000 [c]

[a] Utiliser le préfixe "C" pour indiquer un niveau de classification de CDM.

[b] La condition d'essai de classification n'est pas équivalente à la tension réglée réelle de l'appareil d'essai. Se reporter à 5.6.1 et à l'Annexe H pour de plus amples informations détaillées.

[c] Pour des conditions d'essai au-delà de 1 000 V, et selon la configuration du boîtier de dispositif, les effets de couronne peuvent limiter la tension de prédécharge et le courant de décharge réels.