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colour inside

Digital video interface – Gigabit video interface for multimedia systems

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DIGITAL VIDEO INTERFACE – GIGABIT VIDEO INTERFACE FOR MULTIMEDIA SYSTEMS

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IEC 62889 has been prepared by Technical Area 4: Digital system interfaces and protocols, of IEC Technical Committee 100: Audio, video and multimedia systems and equipment. It is an International Standard.

JEITA CP-6101B served as a basis for the elaboration of this document.

This second edition cancels and replaces the first edition published in 2015. This edition constitutes a technical revision.

This edition includes the following significant technical changes with respect to the previous edition:

a) Addition of a new technology interface, GVIF2.

The text of this International Standard is based on the following documents:

Draft	Report on voting
100/3912/CDV	100/4040/RVC

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/publications.

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- withdrawn, or
- revised.

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INTRODUCTION

This International Standard is based on JEITA CP-6101B: *Digital monitor interface GVIF*, which was originally specified by the Japan Electronics and Information Technology Industries Association (JEITA).

The Gigabit Video InterFace (GVIF) is a serial point-to-point interface supporting uncompressed digital video links that was designed to address the needs of automotive navigation and entertainment systems, etc., to transport baseband digital video information. GVIF applies low-voltage differential signalling (LVDS) technology and makes use of a thin cable consisting of a single shielded twisted pair of conductors that exhibits high noise immunity and low EMI, and is optimized for small size and low weight. GVIF supports display resolutions ranging from WQVGA through WUXGA with a maximum of 24 bits per pixel colour video data, and can transmit a baseband video signal over cable lengths over 10 m. Optionally, GVIF supports audio data transmission and user data transmission.

Gigabit Video InterFace 2(GVIF2) is a baseband transmission method for digital video information that applies serial data transmission technology. In the downstream transmission from GVIF2 TX to GVIF2 RX, the high-bandwidth data for video information (GHDS) and the device control signal (GLDS) are transmitted by using the time-division multiplexing method. In the upstream transmission from GVIF2 RX to GVIF2 TX, the control signal GLUS is transmitted. The upstream transmission and downstream transmission occur in full duplex. Optionally, GVIF2 also supports audio data transmission and user data transmission.

Also optionally, when paired with high-bandwidth ~~data~~ digital content protection (HDCP), the GVIF's standard functions and features address all of the requirements for delivering content-protected video from a source to a video display monitor.

This document describes the GVIF family that consists of GVIF2 in the main body and Annex A, and GVIF in Annex B and Annex C.

GVIF2 has the following features:

- transmission by a differential shielded twisted-pair cable or coaxial cable,
- to enable multiple video and audio content transmission using time-division multiplexing,
- possibility to use audio transmission, bi-direction user communication, and HDCP (high-bandwidth digital content protection) technology (optional),
- availability for daisy chain transmission (optional).

The Association of Radio Industries and Businesses (ARIB) refers to GVIF and GVIF2 in its standard ARIB STD-B21 as being authorized digital video output interfaces.

DIGITAL VIDEO INTERFACE – GIGABIT VIDEO INTERFACE FOR MULTIMEDIA SYSTEMS

1 Scope

This document describes ~~a~~ two serial digital interfaces, Gigabit Video InterFace (GVIF) and Gigabit Video InterFace2 (GVIF2), for the interconnection of digital video equipment. GVIF and GVIF2 are primarily intended to carry high-speed digital video data for general usage and are well suited for multimedia entertainment systems in a vehicle.

This document specifies the physical layer of the interface, including transmission line characteristics and electrical characteristics of transmitters and receivers. Mechanical and physical specifications of connectors are not included.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

~~IEC 62315-1:2003, *DTV profiles for uncompressed digital video interfaces – Part 1: General*~~

ITU-R BT.601-5, *Studio encoding parameters of digital television for standard 4:3 and wide-screen 16:9 aspect ratios*

ITU-R BT.656-5, *Interface for digital component video signals in 525-line and 625-line television systems operating at the 4:2:2 level of Recommendation ITU-R BT.601*

3 Terms, definitions and abbreviated terms

3.1 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminology databases for use in standardization at the following addresses:

- IEC Electropedia: available at https://www.electropedia.org/
- ISO Online browsing platform: available at https://www.iso.org/obp

3.1.1
DE
display enable signal given in IEC 62315-1

3.1.2
HSYNC
display horizontal synchronous signal given in IEC 62315-1

3.1.3
VSYNC
display vertical synchronous signal given in IEC 62315-1

3.1.4
RGB
display red, green, blue colour data input (TX) or output (RX) given in ITU-R BT.601-5 and ITU-R BT.656-5

~~**3.1.5**~~
~~**YU(Cb)V(Cr)**~~
~~display Y, U (Cb), V (Cr) pixel data input (TX) or output (RX) given in ITU-R BT.601-5 and ITU-R BT.656-5~~

3.1.5
CNTL/AUX
downstream user-defined signal or audio enable signal

3.1.6
P[23:0]
digital signal data such as 24-bit colour video data, for example RGB ~~or YU (Cb) V (Cr)~~ data input (TX) or output (RX)

3.1.7
GHDS
GVIF2 High bandwidth DownStream
high-bandwidth downstream content data of the GVIF2 format

3.1.8
GLDS
GVIF2 Low bandwidth DownStream
low-bandwidth downstream control signal data of the GVIF2 format

3.1.9
GLUS
GVIF2 Low bandwidth UpStream
low-bandwidth upstream control signal data of the GVIF2 format

3.1.10
GVIF RX
circuit that receives the serial signal from a shielded-pair transmission line, decodes it and ~~outputs to convert~~ converts it into ~~the~~ a parallel video signal

3.1.11
GVIF TX
circuit that receives the parallel video signal~~,~~ and the control signals, and encodes them into serial data to send a signal by driving a shielded-pair transmission line

3.1.12
GVIF2 RX
circuit that receives the serial signal from a shielded twisted-pair cable or coaxial cable, decodes it and converts it into video and audio/control signals

3.1.13
GVIF2 TX
circuit that receives the video and audio/control signals, encodes them into serial data and sends a signal by driving a shielded twisted-pair cable or coaxial cable

3.1.14
LOS
loss of signal detection ~~signal~~, asserted when the differential input signal at the receiver cannot ~~receive~~ be received

3.1.15
RX front-end
front-end block of receiver side

3.1.16
SDA
serial data down-stream signal

3.1.17
SDATA
GVIF2 serial data signal on coaxial cable transmission

3.1.18
SDATAP
down-stream positive-phase side signal of the differential serial data

3.1.19
SDATAN
down-stream negative-phase side signal of the differential serial data

3.1.20
REF
reference signal

3.1.21
REFRQP
current source positive signal for reference clock request from RX side

3.1.22
REFRQN
current source negative signal for reference clock request from RX side ~~as well as REFRQP~~

3.1.23
SFTCLK
~~**pixel clock**~~
pixel clock for capture of the parallel video data per pixel

3.1.24
TDA
transmit data down-stream user-defined signal

3.1.25
TX front-end
front-end block of transmitter side

3.1.26
UDA
~~user data~~
up-stream user defined ancillary data signal

3.1.27
IRQ
up-stream common-mode reference request current for REFRQP/N

3.1.28
VOS
common-mode voltage amplitude of reference request

3.1.29
VOD
differential voltage amplitude for SDATAP/N

3.1.30
VDD
power supply on the transmitter side

3.1.31
V_SDATAP
single-ended voltage of SDATAP

3.1.32
V_SDATAN
single-ended voltage of SDATAN

3.1.33
TP1
~~transmitter end point for~~ test point of a downstream eye mask specification

3.1.34
TP2
test point of an upstream eye mask specification

3.1.35
normalized differential voltage
voltage of transmitter output point

3.1.36
UI
normalized time unit interval of transmitter output point

3.1.37
WSYNC
word synchronized signal

3.2 Abbreviated terms

AC alternating current
DC direct current
EMI electro-magnetic interference
GVIF Gigabit Video InterFace
HDCP high-bandwidth digital content protection
LSB least significant bit
LVDS low voltage differential signalling
MSB most significant bit
PRBS pseudo random binary sequence

4 Architecture

The GVIF2 has a higher capability multimedia interface and is considered as the next generation of GVIF, which is described in Annex B and Annex C.

The GVIF2 transmission line is a shielded twisted-pair cable with the differential characteristic impedance Z0_diff or a coaxial cable with the characteristic impedance Z0_coax, and is

connected to GVIF2 RX and GVIF2 TX, with an AC coupling capacitor, and high-frequency terminated resistor (see Figure 1). The signal path of the transmission line of GVIF2 is DC isolated from both GVIF2 TX and GVIF2 RX. The shield of the transmission line of GVIF2 is connected to the GND of the TX circuit and of the RX circuit.

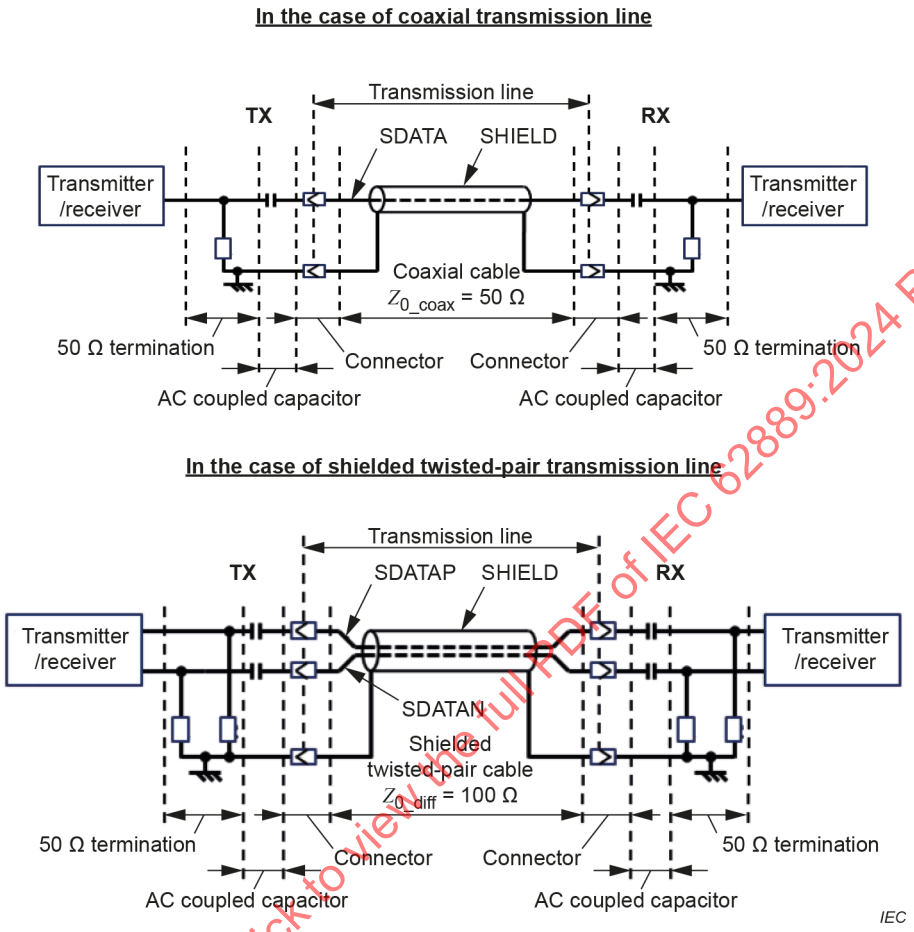

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Figure 1 – Architecture of the GVIF2

5 Electrical characteristics

5.1 General

AC specifications described in below shall be satisfied. GVIF2 does not specify DC specifications because the transmission architecture of GVIF2 is a complete AC coupling.

5.2 AC electrical specifications

The AC electrical specifications of the transmitter and receiver side are given in Table 1. The definition of voltage levels are shown in Figure 2, and Figure 3 and Figure 4 show a downstream eye mask specification at TP1 and an upstream eye mask specification at TP2 for GVIF2.

Table 1 – AC electrical specification of GVIF2

	Downstream bit rate			Upstream bit rate
	Fdownstream_1	Fdownstream_2	Fdownstream_3	Fupstream
	Gbit/s	Gbit/s	Gbit/s	Mbit/s
Minimum	2,16	3,24	4,32	9,0
Maximum	2,4	3,6	4,8	10,0
Fupstream = Fdownstream_1/240 or Fupstream = Fdownstream_2/360 or Fupstream = Fdownstream_3/480				
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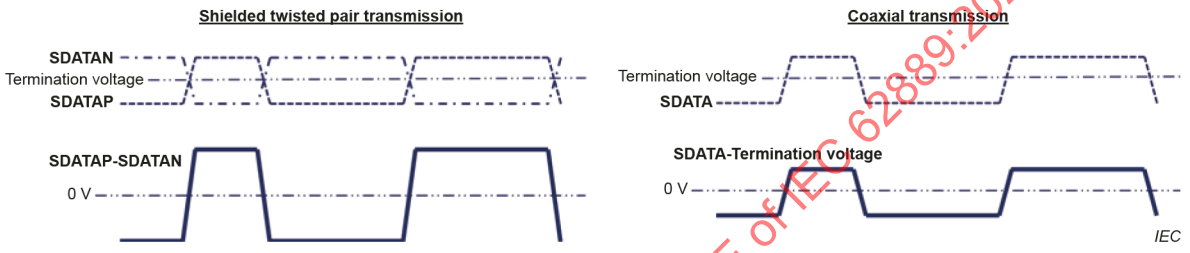

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Figure 2 – Level definition of GVIF2

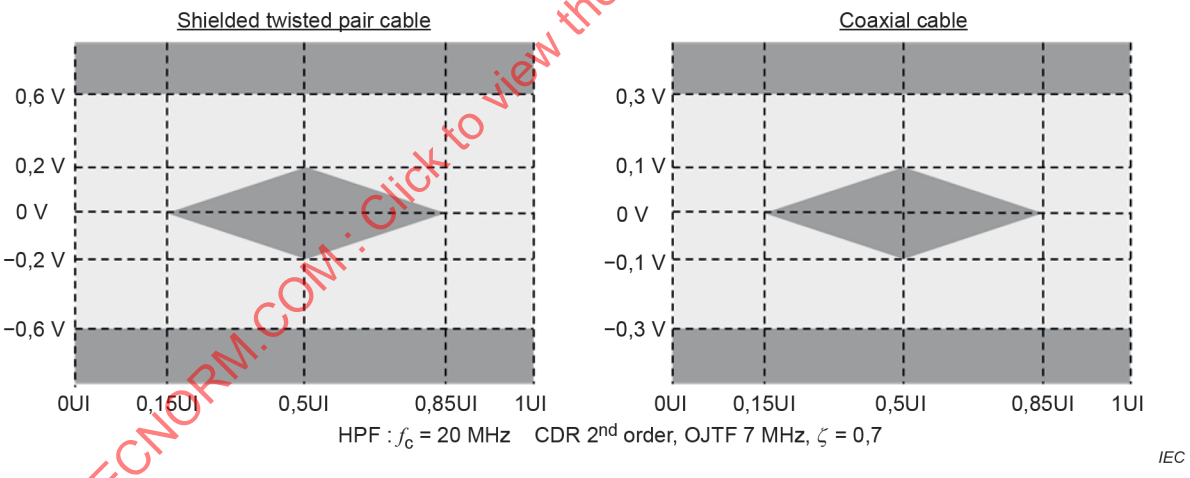

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Figure 3 – GVIF2 downstream eye mask (at TP1)

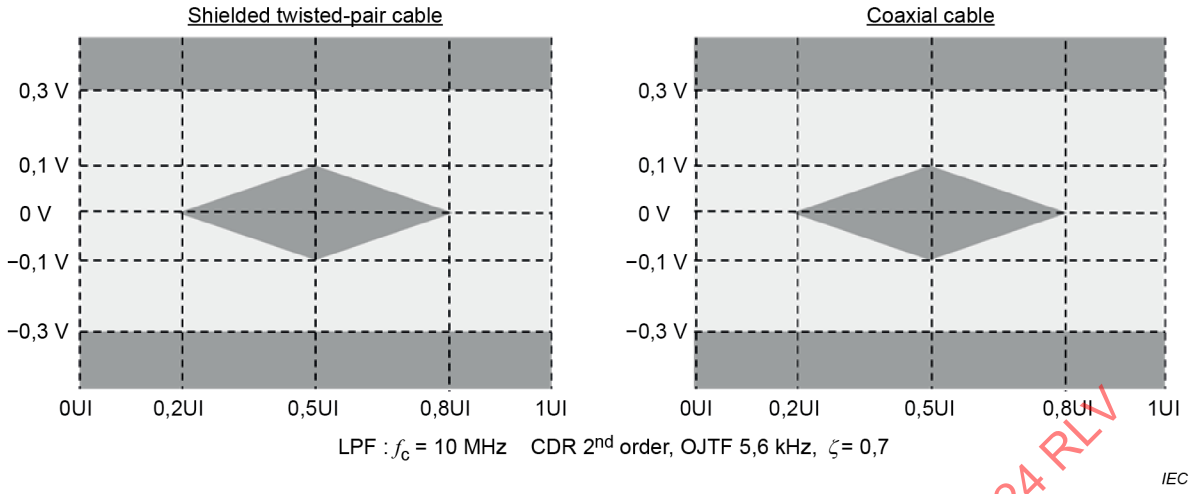

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Figure 4 – GVIF2 upstream eye mask (at TP2)

6 Front-end

6.1.1 General

The front-end block diagram of GVIF2 is shown in Figure 5.

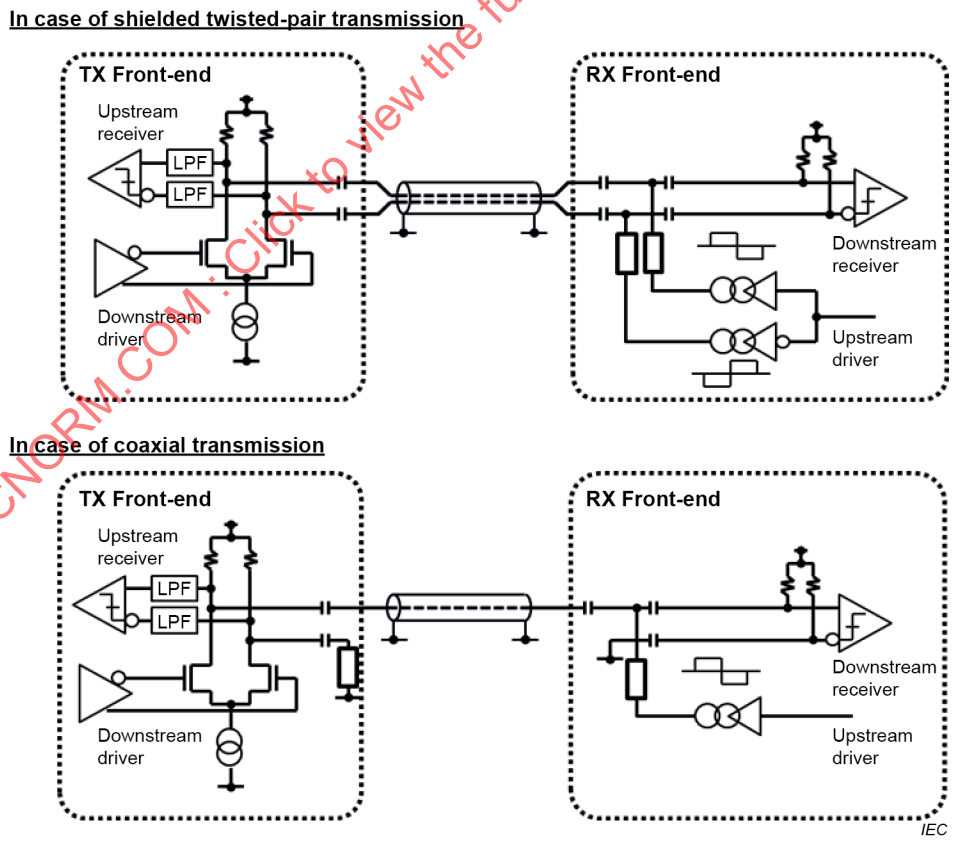

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Figure 5 – Front-end block diagram of GVIF2

6.1.2 TX Front-end

The GVIF2 TX front end consists of AC coupling capacitors, termination resistors, a downstream driver, an upstream receiver, and connectors. The termination resistors, as the load of the differential current from the downstream driver, generate the downstream signal voltage, and become the high-frequency termination of the transmission line. The upstream receiver reproduces the data extracted by the low-pass filter (LPF) from the upstream signal transmitted by the RX.

6.1.3 RX Front-end

The GVIF2 RX front end consists of AC coupling capacitors, termination resistors, a downstream receiver and an upstream driver. The downstream receiver reproduces the data from the downstream signal which is transmitted from the TX and extracted by the high-pass filter (HPF), which consists of the AC coupling capacitors and the termination resistors. The upstream driver drives the upstream signal to the transmission line via the LPF. The upstream signal is in frequency synchronization with the downstream signal, and the transmitted rate is 10 Mbit/s at maximum, which is proportional to the downstream rate.

6.1.4 Configuration block diagram

Downstream signal is GHDS and GLDS encoded in the downstream code, and the transmission rate shall be selected from 2,4 Gbit/s, 3,6 Gbit/s, or 4,8 Gbit/s according to the bandwidth required for GHDS.

GHDS shall be set by a time-division multiplexing in DATA SLOT units.

GHDS may use multiple video (and audio) contents transmission (optional, see Annex A).

Upstream signal shall be GLUS-encoded in upstream code.

Upstream and downstream shall be transmitted simultaneously (full duplex) by frequency division.

The GVIF2 configuration block diagram data mapping is shown in Figure 6.

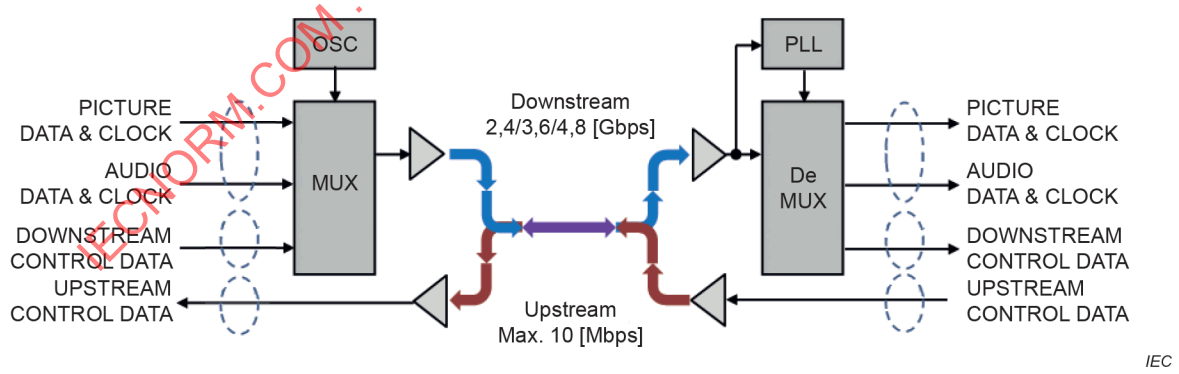

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Figure 6 – GVIF2 configuration block diagram Data mapping

6.1.5 Data mapping

6.1.5.1 RGB888 data mapping for GHDS

RGB888 data and synchronization signals VSYNC/HSYNC/DE shall be mapped into GHDS as shown in Figure 7.

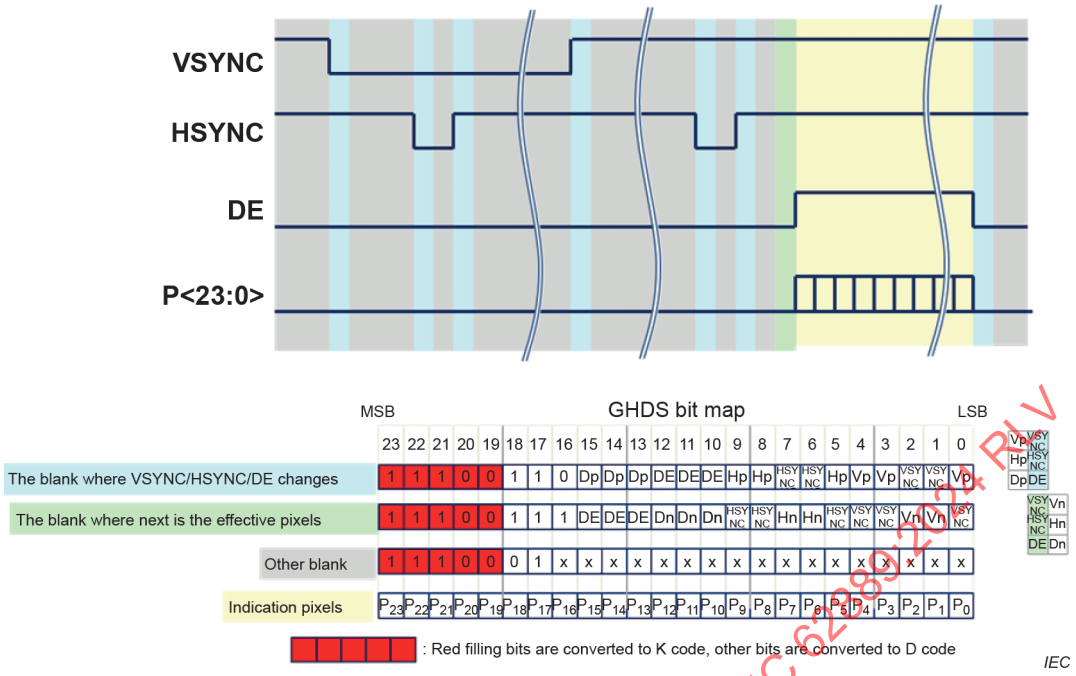

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Figure 7 – GVIF2 RGB888 data mapping

6.1.5.2 Mapping of content for other formats (optional)

MAINDATA, MAINCTRL, SUBDATA can be mapped into GHDS following the agreement of coordination between GVIF2 TX and GVIF2 RX, as shown in Figure 8. It is recommended that video pixel data be mapped into MAINDATA, video synchronization signals be mapped into MAINCTRL, and audio signals (optional) be mapped into SUBDATA.

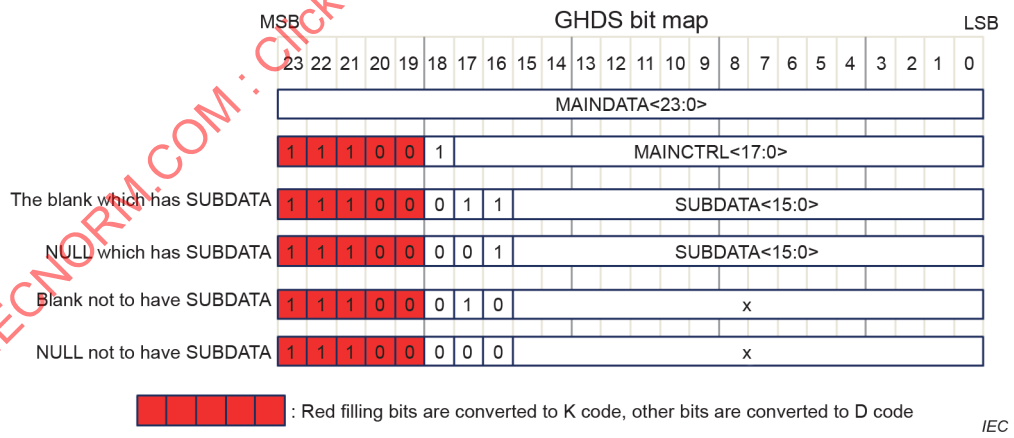

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Figure 8 – GVIF2 mapping for general content data(optional)

Bi-directional communication signals between GVIF2 TX and GVIF2 RX, such as UART, can be mapped into GLDS and GLUS (optional).

Certification data for HDMI (HDCP) is recommended to be mapped into SUBDATA, GLDS, GLUS, and a part of GHDS (optional).

7 Transition state link

The transition state diagram of GVIF2 TX and GVIF2 RX is shown in Figure 9.

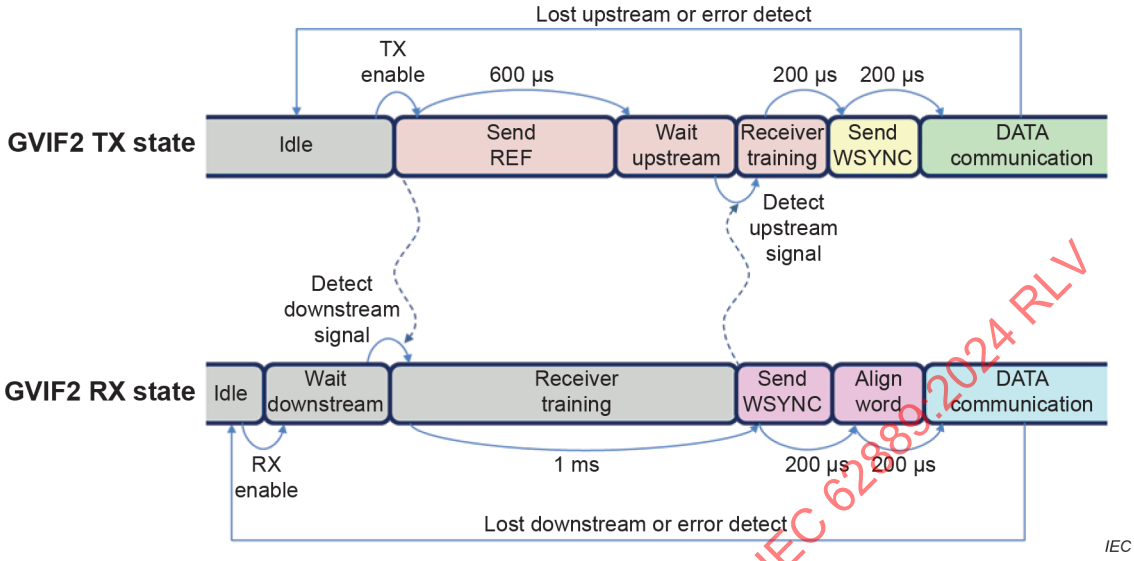

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Figure 9 – Transaction state diagram of GVIF2

In the GVIF2 TX connected to the GVIF2 RX, there are several states including a state without down-stream signal (Idle), states transmitting a REF signal (Send REF, Wait Upstream, Receiver Training), a state transmitting a SYNC signal (Send WSYNC), and a normal downstream transmission state. While it shall transit from Idle to Send REF when the TX circuit is activated, and shall transit from Wait Upstream to Receiver Training when the upstream signal is detected, the other transitions shall occur unconditionally in the specified time. If the upstream signal is not detected in the normal downstream transmission state or an error is detected in the upstream signal, it shall transit to Idle.

In the GVIF2 RX connected to the GVIF2 TX, there are several states, including a state without upstream signal (Idle, Wait Downstream, Receiver Training), states transmitting a SYNC signal (Send WSYNC, Align Word), and a normal upstream transmission state. While it shall transit from Idle to Waite Downstream when the RX circuit is activated, and shall transit from Wait Downstream to Receiver Training when the down-stream signal is detected, the other transitions shall occur unconditionally in the specified time. If the downstream signal is not detected in the normal upstream transmission state, or an error is detected in the down-stream signal, it shall transit to Idle.

The downstream REF and WSYNC signals output from the GVIF2 TX shall be the encoded GHDS and GLDS (see Figure 10).

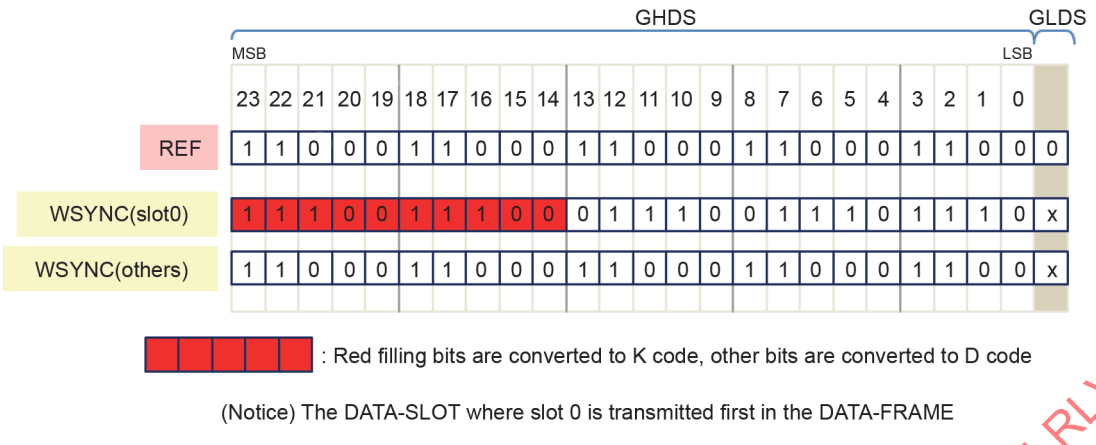

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Figure 10 – REF and WSYNC signals of GVIF2 downstream

The upstream WSYNC signal output from GVIF2-RX shall be the encoded GLUS in Figure 11.

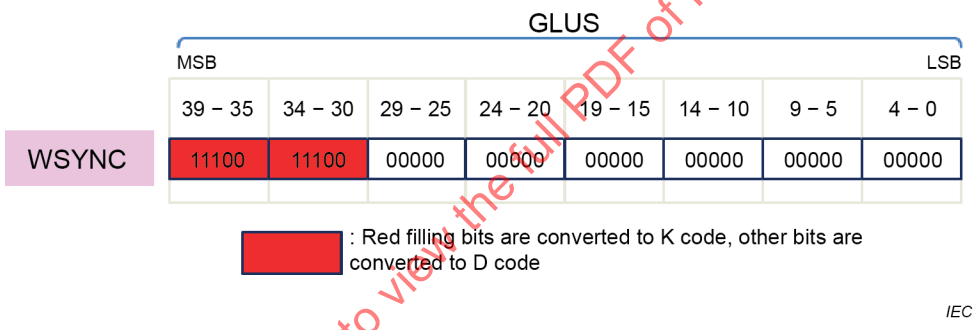

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Figure 11 – WSYNC signal of upstream

8 Protocol

8.1 Downstream encoder

8.1.1 General

The downstream encoder shall perform operations of GHDS and GLDS concatenation, scrambling, and the 5B/6B conversion shown in Figure 12.

8.1.2 GHDS and GLDS concatenation

The 25-bit word shall be generated with 24-bit GHDS on the MSB side and 1-bit GLDS on the LSB side.

8.1.3 Scrambler

The part of word column which is converted to D code shall be scrambled by PRBS31 (pseudorandom binary sequence 31).

8.1.4 5B/6B conversion

The 25-bit word shall be divided into 5 bits and each 5-bit data shall be converted to the 6-bit D code or K code in accordance with Table 2. The generated 30-bit downstream data shall be converted to serial data and shall be transmitted to the RX leading with the MSB.

Table 2 – 5B/6B conversion

Input		RD = −1	RD = +1		Input		RD = −1	RD = +1
Code	EDCBA	abcdei			Code	EDCBA	abcdei	
D.00	00000	100111	011000		D.16	10000	011011	100100
D.01	00001	011101	100010		D.17	10001	100011	
D.02	00010	101101	010010		D.18	10010	010011	
D.03	00011	110001			D.19	10011	110010	
D.04	00100	110101	001010		D.20	10100	001011	
D.05	00101	101001			D.21	10101	101010	
D.06	00110	011001			D.22	10110	011010	
D.07	00111	111000	000111		D.23	10111	111010	000101
D.08	01000	111001	000110		D.24	11000	110011	001100
D.09	01001	100101			D.25	11001	100110	
D.10	01010	010101			D.26	11010	010110	
D.11	01011	110100			D.27	11011	110110	001001
D.12	01100	001101			D.28	11100	001110	
D.13	01101	101100			D.29	11101	101110	010001
D.14	01110	011100			D.30	11110	011110	100001
D.15	01111	010111	101000		D.31	11111	101011	010100
					K.28	11100	001111	110000

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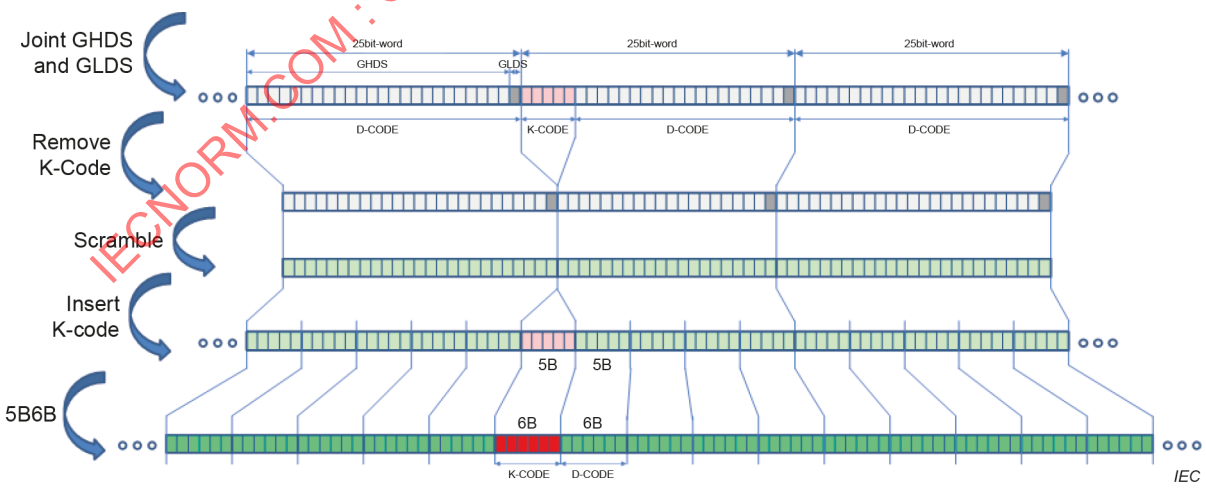

Reproduced from JEITA CP-6101B, Figure D.1-1, with permission from JEITA.

Figure 12 – Downstream encoding

8.2 Downstream decoder

The decoder shall perform reverse operation of the downstream encoder, that is 6-bit to 5-bit reverse conversion, descrambling, and GHDS/GLDS decomposition, as shown in Figure 13.

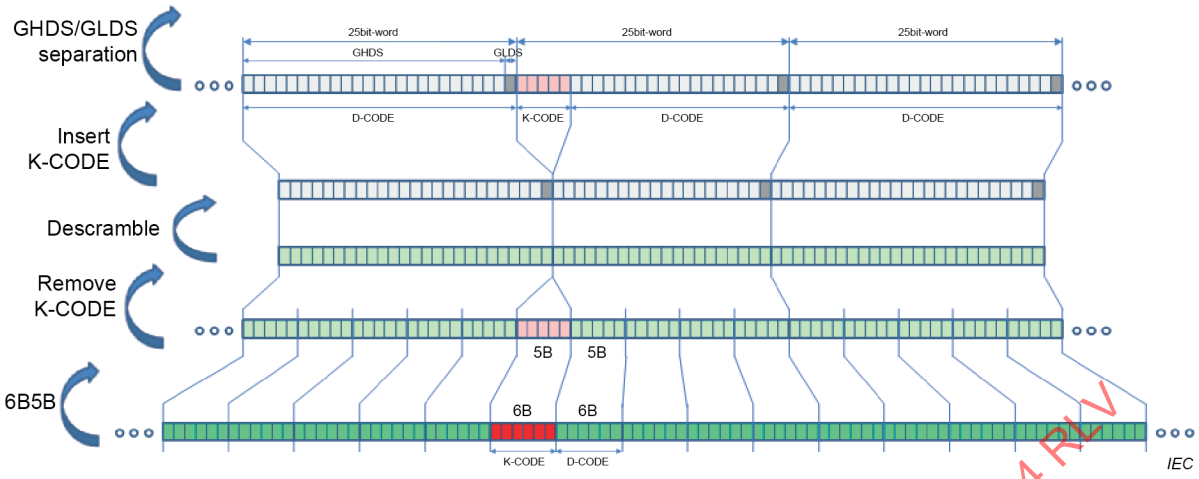

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Figure 13 – Downstream decoding

8.3 Upstream encoder

8.3.1 GLUS concatenation

GLUS data includes 4-bit length GLUS0, updated 8 times, 1-bit length GLUS1 and GLUS2, updated twice, and 1-bit length GLUS3, GLUS4, GLUS5 and CHK (checksum), updated once, for every 4,8 µs. The GLUS data shall be compiled as shown in the Figure 14 to generate a 40-bit GLUS word.

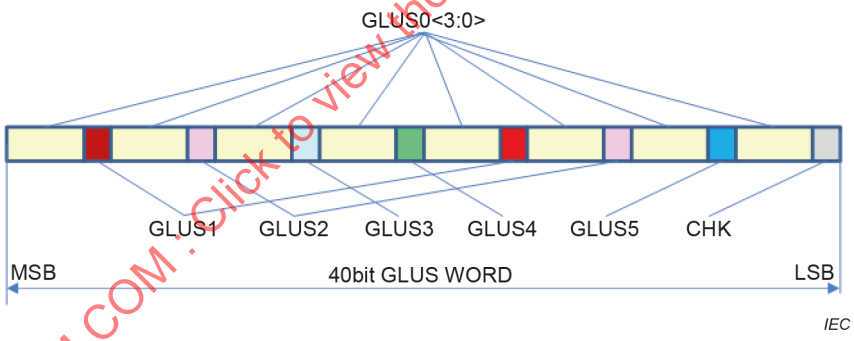

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Figure 14 – GLUS word structure

8.3.2 Scrambler

The part of word column which is converted to D code shall be scrambled by PRBS7 (pseudorandom binary sequence 7).

8.3.3 5B/6B conversion

The 40-bit word is divided into 5 bits and each 5-bit data is converted into the 6-bit D code, in accordance with Table 2. The generated 48-bit length upstream data is converted to serial data and shall be transmitted to GVIF2 TX, with a leading MSB.

8.3.4 Upstream decoder

The decoder shall perform the reverse operation of the upstream encoder, which is 6-bit to 5-bit reverse conversion, descrambling, and decomposition into GLUS 0 to 5.

9 Transmission system and transmission line of electrical characteristics

The transmission line characteristics of GVIF2 are defined by the TP1 and TP2 (test points) in Figure 15.

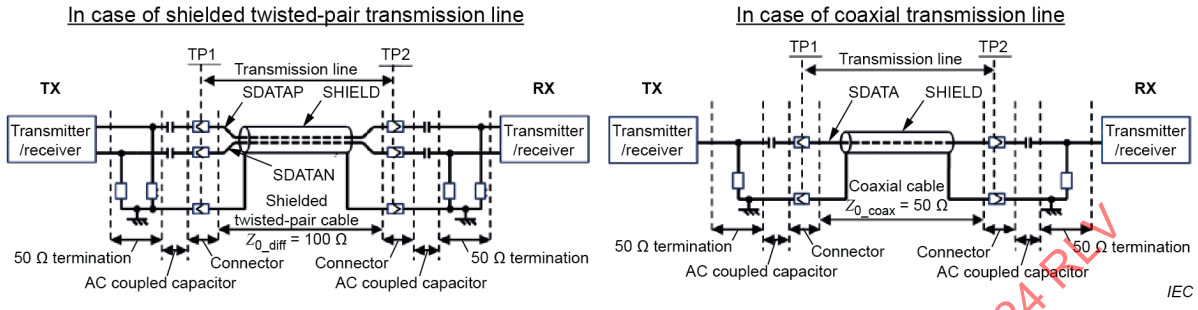

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Figure 15 – Test points of GVIF2

The shielded twisted-pair cable and coaxial cable (TP1 to TP2) should meet the S21 template in Figure 16.

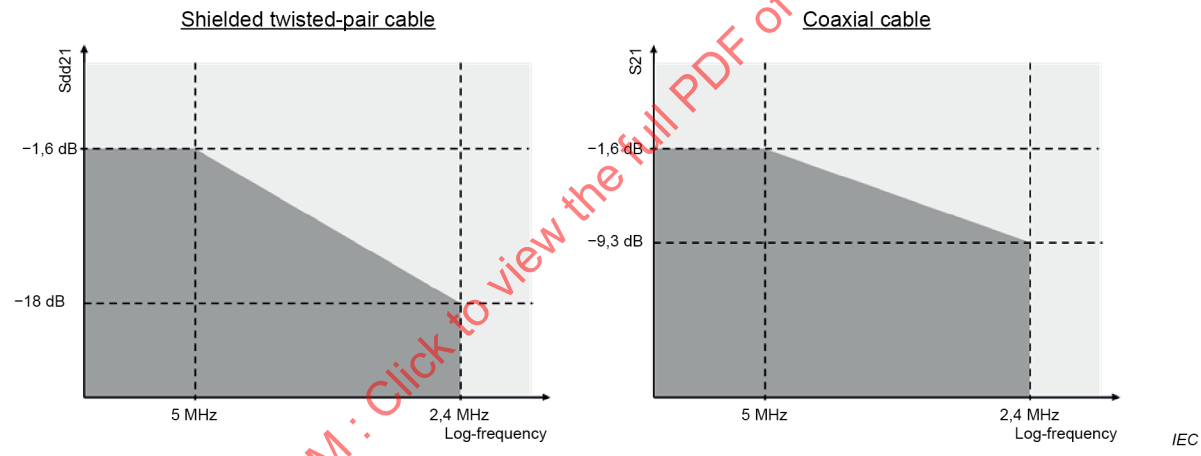

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Figure 16 – S21 template for GVIF2 transmission line

Annex A
(informative)

GVIF2 multiple contents transmission

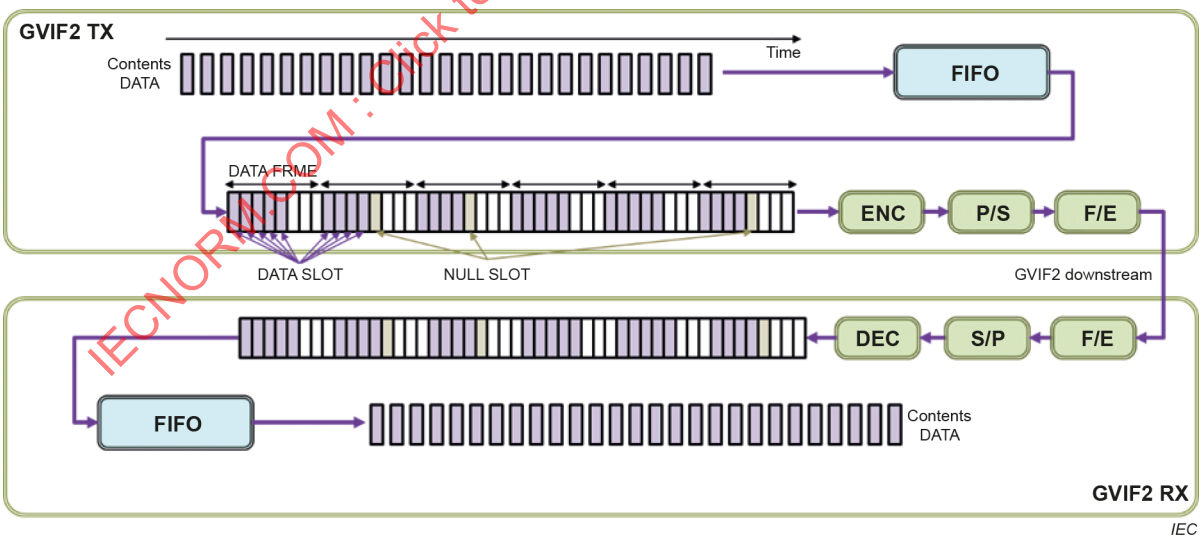
The GVIF2 downstream signal is in the unit of DATA FRAME, and the DATA FRAME has the number of DATA SLOTs specified in Table A.1. The DATA SLOT is one word (24 bits) of GHDS, in which video (and audio: optional) contents are mapped.

Data of different contents can be mapped to each DATA SLOT. In GVIF2 TX, each content is assigned the required number (fixed number) of DATA SLOTs to each DATA FRAME according to its content data bandwidth. Content data is packed into a DATA SLOT through data FIFO, but if the data FIFO is empty, the assigned DATA SLOT is padded with NULL SLOT. In GVIF2 RX, the content to be used for display is extracted from the assigned DATA SLOT and stored in the data FIFO shown in Figure A.1 and Figure A.2.

By stacking TX and RX of GVIF2 in multiple stages, it is possible to form a daisy chain that simultaneously transmits multiple contents with a shielded twisted-pair cable or a single coaxial cable (optional).

Table A.1 – GVIF2 data rate of transmission and number of the DATA SLOT

Downstream bit rate	DATA SLOT/DATA FRAME
2,4 Gbit/s	8
3,6 Gbit/s	12
4,8 Gbit/s	16
Reproduced from JEITA CP-6101B, Table 3-1, with permission from JEITA.	



Reproduced from JEITA CP-6101B, Figure 3-5, with permission from JEITA.

Figure A.1 – GVIF2 transmission for single content

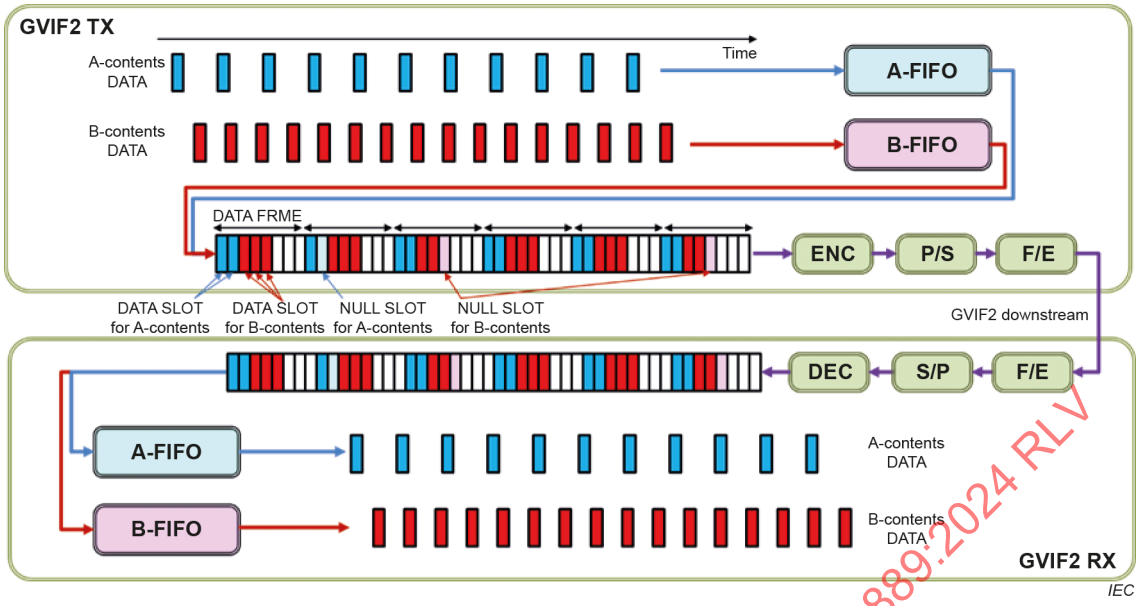


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Figure A.2 – GVIF2 multiplex transmission for multiple contents

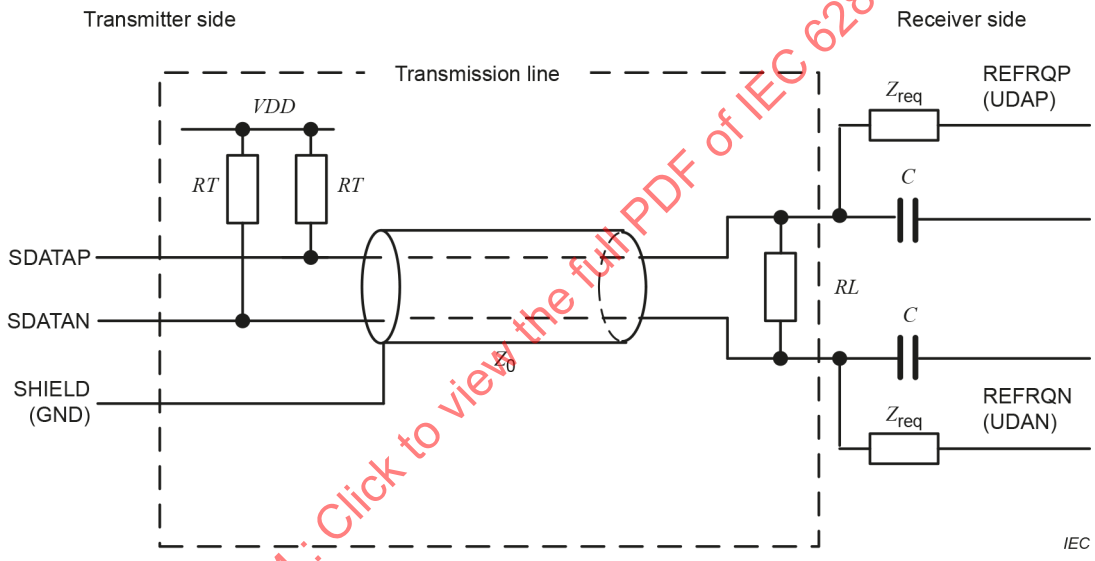
Annex B
(normative)

GVIF standard specification

B.1 Architecture

Figure B.1 illustrates the architecture of the GVIF. The fundamental operation of the GVIF is a simultaneous bi-directional data transmission technology, in which the low-voltage differential signal is transmitted down from the transmitter side to the receiver side, and the common-mode voltage signal is transmitted up from the receiver side to the transmitter side through a shielded twisted differential pair cable.

The shielded twisted-pair transmission line has the characteristic impedance Z_0 (see Figure B.1), the line is terminated to VDD by RT of (50 ± 15) Ω on the transmitter side, and is terminated carrying differential data in RL of (100 ± 5) Ω on the receiver side.



where

RT are the pull-up terminated load resistors on the transmitter side (50 ± 15) Ω;

Z_0 is the characteristic impedance of the shielded twisted-pair transmission line;

RL is the terminated resistor between differential data lines on the receiver side (100 ± 5) Ω;

C are AC coupling capacitors.

SDATAP/SDATAN are the downstream positive and negative phases side signals carrying differential serial data.

REFRQP (UDAP)/REFRQN (UDAN) is the upstream REFREQ common-mode current signal or UDA common-mode current user defined data signal. UDAP/UDAN are optional.

SHIELD (GND) is the GND and shielded ground for cable.

Z_{req} is a blocking filter for the upstream signal. It can use resistors or inductors depending on the system implementation.

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Figure B.1 – Architecture of the GVIF

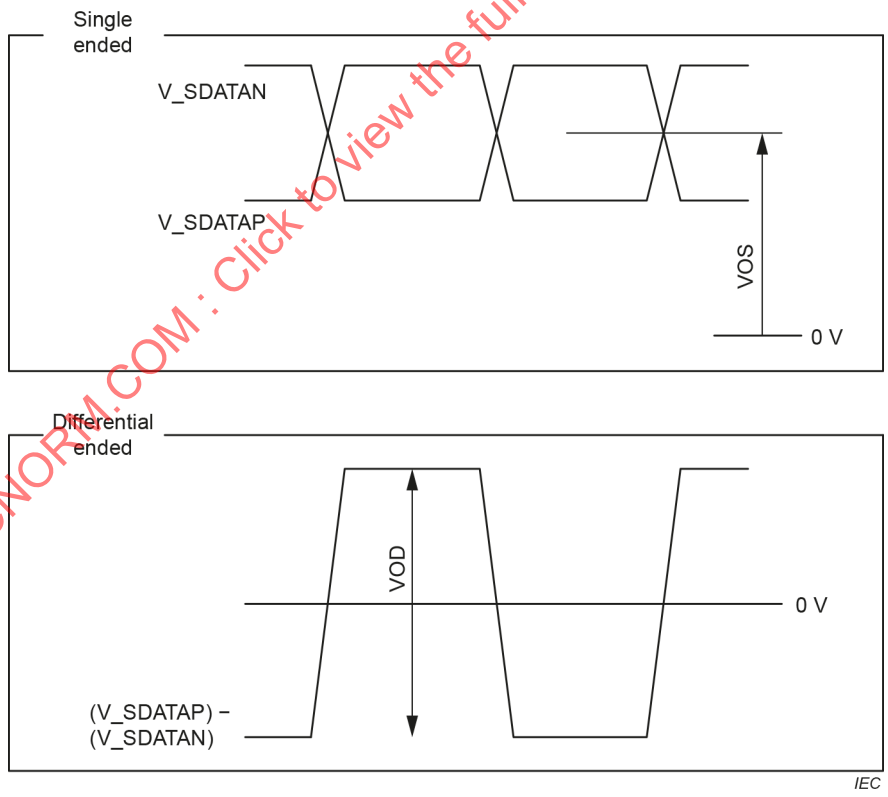
B.2 Electrical characteristics

B.2.1 DC electrical specifications

The DC electrical specifications of the transmitter side are shown in Table B.1 and Figure B.2, and the DC electrical specifications of the receiver side are shown in Table B.2.

Table B.1 – DC electrical specifications of the transmitter

	~~Differential output peak to peak voltage (SDATAP/N)~~ VOD mV	~~Common mode voltage (SDATAP/N)~~ VOS V		Input REFRQ assert current (SDATAP/N) mA	Input REFRQ de-assert current (SDATAP/N) mA
	Condition: RT = 50 Ω RL = 100 Ω	Condition: RT = 50 Ω RL = 100 Ω IRQ = 0 mA	Condition: RT = 50 Ω RL = 100 Ω IRQ = 11 mA		
Minimum	690	VDD − 0,55	VDD − 1,2		−2,0
Typical	800				
Maximum	910	VDD − 0,35	VDD − 0,8	−7,3	
Reproduced, with modifications, from JEITA CP-6101B, Table 4-1, with permission from JEITA.					



Reproduced, with modifications, from JEITA CP-6101B, Figure 4-1, with permission from JEITA.

Figure B.2 – VOD and VOS diagrams

Table B.2 – DC electrical specifications of the receiver

	Output HIGH current (REFRQP/N) mA	Output LOW current (REFRQP/N) mA
Minimum	−0,1	7,4
Maximum	0,1	11
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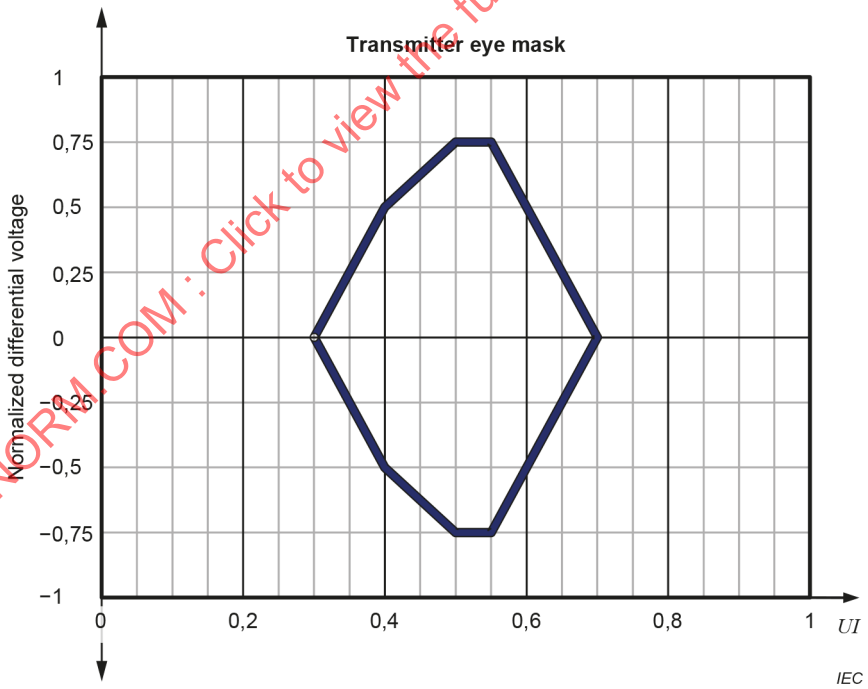
B.2.2 AC electrical specifications

The AC electrical specifications of the transmitter side are shown in Table B.3, and Figure B.3 shows a transmitter end point eye specification (TP1). The AC electrical specifications of the receiver side are shown in Table B.4.

Table B.3 – AC electrical specifications of the transmitter

	SFTCLK frequency MHz	UDA data rate (upstream) Mbit/s	SFTCLK duty factor %
Minimum	7,6	0,01	40
Maximum	160	2,41	60



Reproduced, with modifications, from JEITA CP-6101B, Figure 4-2, with permission from JEITA.

Figure B.3 – Transmitter eye mask specifications (TP1)

Table B.4 – AC electrical specifications of the receiver

	SFTCLK frequency MHz	UDA data rate (upstream) Mbit/s
Minimum	7,6	0,01
Maximum	160	2,41

B.3 Front-end

B.3.1 General

The front-end block diagram of GVIF is shown in Figure B.4.

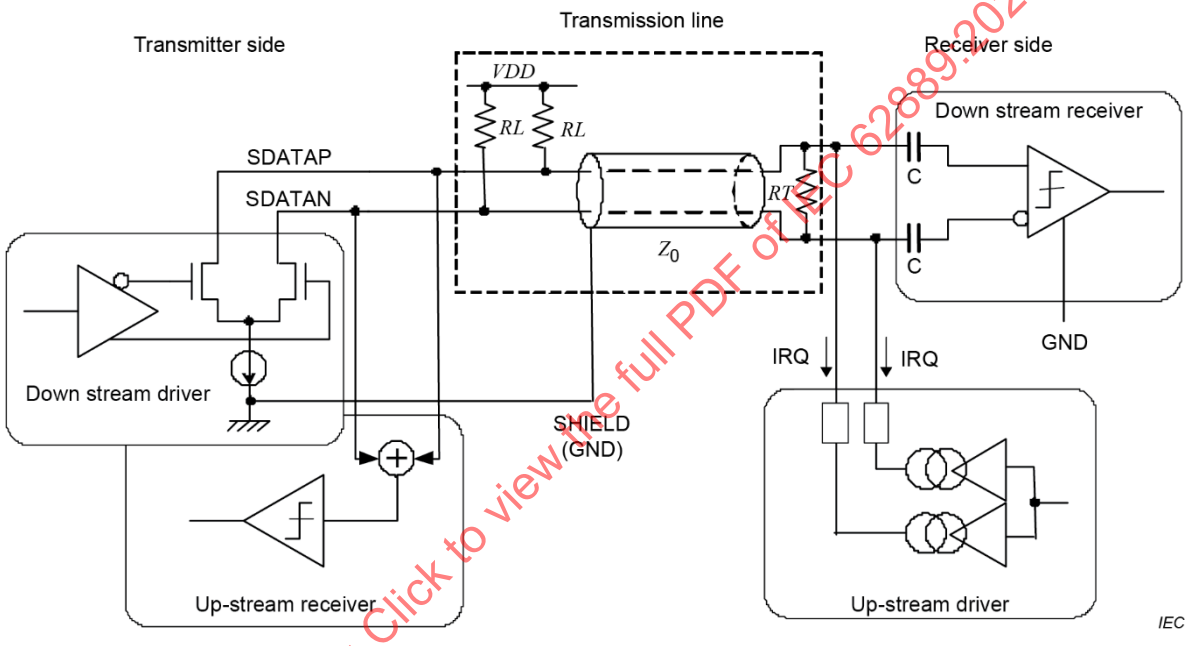


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Figure B.4 – Front-end block diagram

B.3.2 TX front-end

The TX front-end consists of a termination circuit, a downstream driver and an upstream receiver. The termination circuit consists of 2 resistors RL, and the SDATAP/N differential signal is pulled up to voltage reference (VDD) with a (50 ± 15) Ω resistor. The downstream driver consists of a differential current output circuit that is driven by the serial signal from the encoder. The up-stream receiver detects the common-mode signal which RX sends through the shielded twisted-pair line. The input to the downstream driver has two modes. One is the serialized actual encoded video data input mode and the other is the reference clock signal for REFREQ handshake input mode. These two modes activate depending on the common-mode signal level. The common-mode signal level is normally high. When a long low-level pulse is detected, the upstream receiver activates the REFREQ signal, and changes a mode of the encoder into the reference clock mode. In the case of the optional upstream user data transmission, the upstream receiver outputs the common-mode voltage as a UDA signal by using binary digital data sent to the encoder. In this case, the upper limit of the low-pulse time is 100 µs.

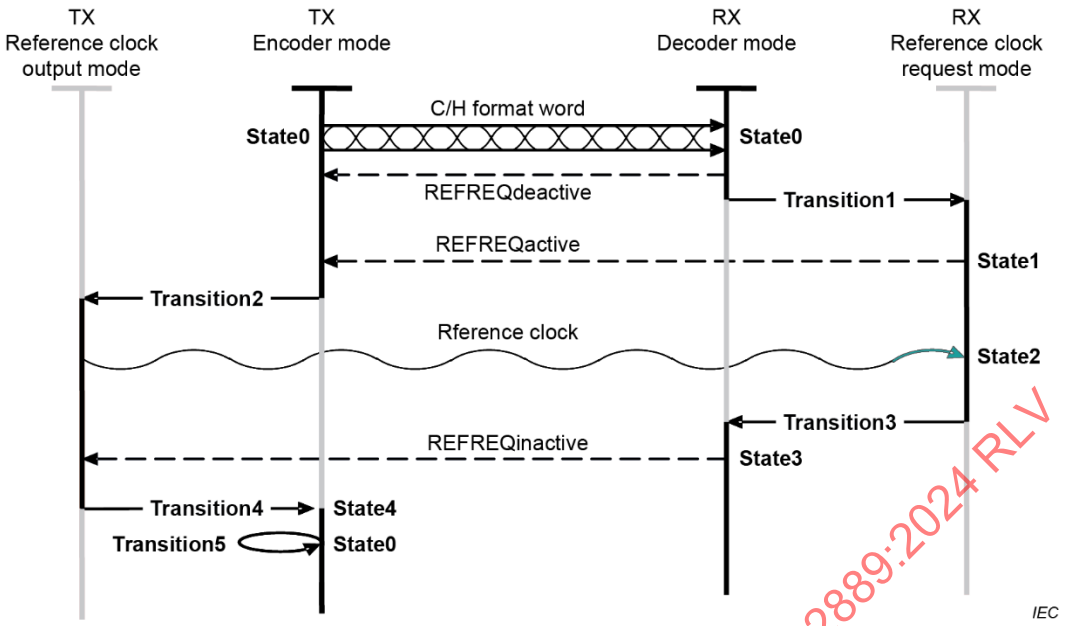
B.3.3 RX front-end

The RX front-end consists of AC capacitors, a termination resistor RT (100 ± 5) Ω, a downstream receiver and an upstream driver. The downstream receiver consists of a differential input detection circuit, which receives the transmission potential differential signal through the shielded twisted-pair line. The upstream driver drives the upstream transmission signal applying a current through the termination resistor RX through the shielded twisted-pair transmission line. A recommended transmission system and transmission line for electrical characteristics is specified in Clause B.2.

B.4 Transition state link

The transition state link of GVIF shall meet the procedure described below.

There are two states in the connection link between GVIF TX and GVIF RX. One is the state transmitting differential signal with a reference clock, the other is the state transmitting the H-format word or the C-format word. In the former state, the TX encoder is in the reference clock output mode and the RX decoder is in the reference clock request mode. In the latter state, the TX encoder changes into the encoder mode and the RX decoder changes into the decoder mode. The state transition switching diagram of the encoder and the decoder is shown in Figure B.5.



State0 (normal)	:	The C/H format word is transmitted down from the TX in the encoder mode to the RX, and the deactivation signal REFREQ is transmitted from the RX in the decoder mode to the TX.
Transition1	:	Transition to the reference clock request mode after finding an irregular HSYNC when the RX decodes.
State1	:	The RX transmits up the activate signal REFREQ.
Transition2	:	The TX transits to the reference clock output mode when the activate signal REFREQ is detected.
State2	:	The TX transmits down the reference clock, and the RX adjusts the internal sampling clock.
Transition3	:	The RX transits to the decoder mode after the internal sampling clock adjustment.
State3	:	The RX transmits up the inactivate signal REFREQ.
Transition4	:	The TX transits to the encoder mode when the inactivate signal REFREQ is detected.
State4	:	P[23:0] transmits continuously the H/C format word equivalent all zero until the TX transmits (VSYNX, HSYNC) (1,1) → (1,0) 60 times.
Transition5	:	Return to normal when the signal has been transmitted 60 times.

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Figure B.5 – Transition state link

B.5 Protocol

B.5.1 General

The encoder encodes the 30 bits of data (P[23:0], HSYNC, VSYNC, DE, CNTL, SDA and TDA) in synchronization with the input of SFTCLK, and outputs 1 bit of the serial signal S to the TX front-end.

To ensure the DC balance data and a reasonable transition, it is required to generate a synchronization pattern for each word in synchronization with the falling edge of HSYNC at the receiver.

B.5.2 Encoder

The encoder encodes the full 30 bits of input data (P[23:0], HSYNC, VSYNC, DE, CNTRL, SDA and TDA) synchronized with SFTCLK, and outputs a 1-bit serial signal S to the TX front-end. The signal is coded after dividing into the following data:

a) Broadband data P[23:0] (24 bits), no transition data.

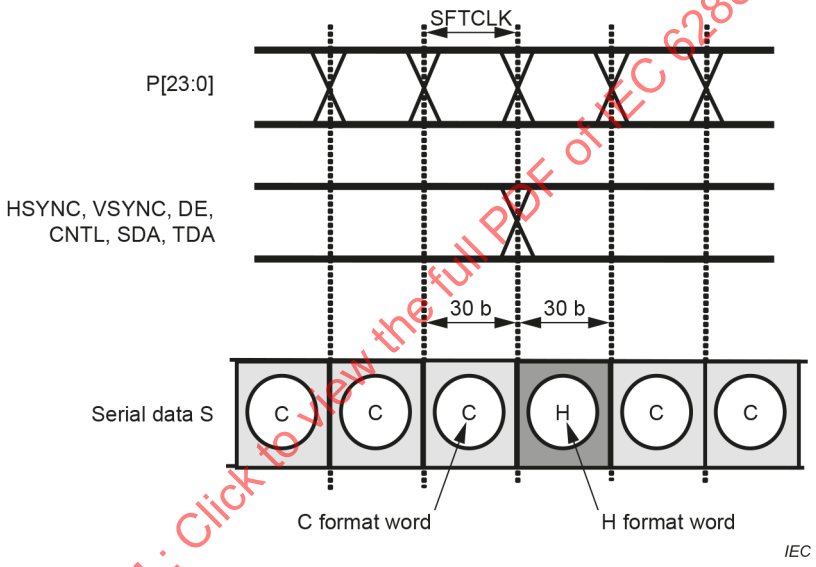
b) Time mark data HSYNC, VSYNC, DE, CNTL, SDA and TDA (6 bits).

Transition frequency of the signal is limited by the logical specification coding.

The broadband data are normally converted to 1-bit data, but in the case of the time mark data, the transition is converted to 1-bit data. When there is no transition in the time mark data, the broadband data are converted to the C format with 20 % overhead. When there is a time mark transition, the broadband data are converted to the H format with a 6-bit header and 24-bit broadband data.

The broadband data and the time mark data are output as a serial signal S led by the MSB after conversion into a 30-bit length C-format word or H-format word.

The C-format word is used when there is no time mark data transition at the previous pixel clock cycle, and the H-format word is used when there is/are one or more time mark data transition(s) at the previous pixel clock cycle (see Figure B.6).



Reproduced from JEITA CP-6101B, Figure B-1, with permission from JEITA.

Figure B.6 – Encoder output diagram

The C-format word consists of the combined six codes of 5 bits which is generated by the 4B/5B conversion (see Table B.5), braking the broadband data P[23:0] by 4 bits (see Figure B.7).

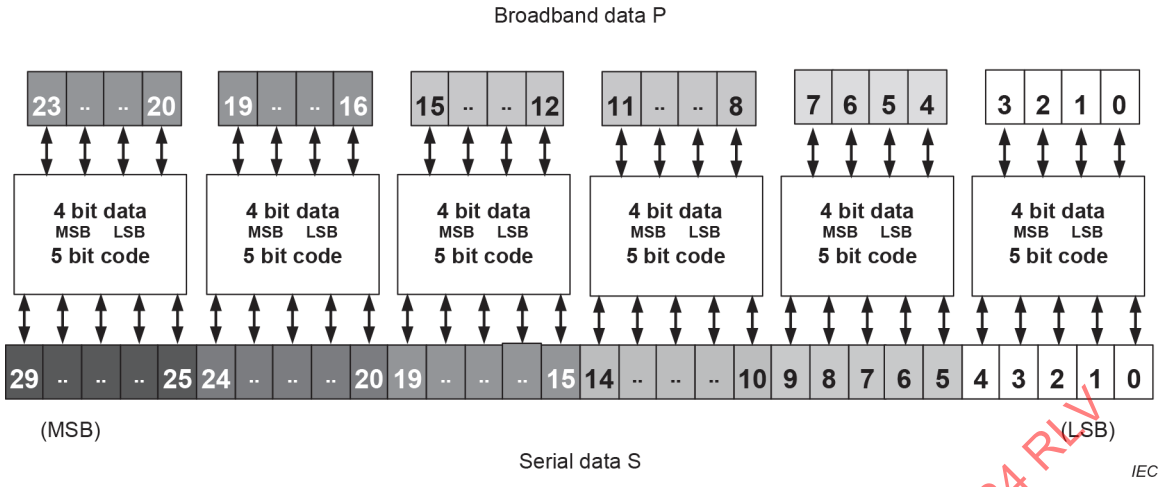


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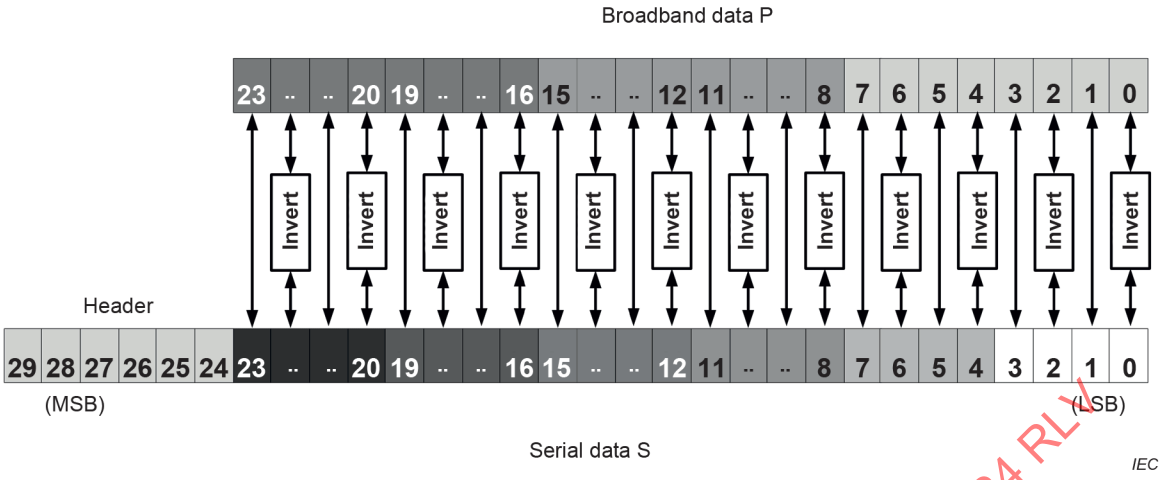
Figure B.7 – C-format word

Table B.5 – 4B/5B conversion

4-bit data MSB – LSB	5-bit code MSB – LSB	4-bit data MSB – LSB	5-bit code MSB – LSB
"0 0 0 0"	"0 0 1 1 0"	"1 0 0 0"	"1 0 0 1 0"
"0 0 0 1"	"0 0 1 1 1"	"1 0 0 1"	"1 0 0 1 1"
"0 0 1 0"	"0 1 0 0 1"	"1 0 1 0"	"1 0 1 0 0"
"0 0 1 1"	"0 1 0 1 0"	"1 0 1 1"	"1 0 1 0 1"
"0 1 0 0"	"0 1 0 1 1"	"1 1 0 0"	"1 0 1 1 0"
"0 1 0 1"	"0 1 1 0 1"	"1 1 0 1"	"1 1 0 0 1"
"0 1 1 0"	"0 1 1 1 0"	"1 1 1 0"	"1 1 0 1 0"
"0 1 1 1"	"0 1 1 1 1"	"1 1 1 1"	"1 1 1 0 0"
Reproduced from JEITA CP-6101B, Table B-1, with permission from JEITA.			

The H format is generated by a combination of the 24-bit broadband data P[23:0] with a 6-bit header that indicates the transition state of a time mark (see Figure B.8). The positions of even numbers of the broadband data P are inverted in the serial data S. The structure of the header is shown in Table B.6.



Reproduced from JEITA CP-6101B, Figure B-3, with permission from JEITA.

Figure B.8 – H-format word

Table B.6 – VSYNC, HSYNC, DE, CNTL/AUX, SDA, TDA transition and the corresponding header

	Transition signal	Header bit array	Remark
a	VSYNC, HSYNC	"1 0 0 0 V H"	V and H are the VSYNC inversion value and the HSYNC value after transition.
b	DE, CNTL/AUX	"0 1 1 1 D C"	D and C are the DE and CNTL values after transition.
c	SDA, TDA	"1 1 1 1 S T"	S and T are the SDA and TDA values after transition.
Transition between the signals simultaneously among a, b and c shall not be permitted. Reproduced, with modifications, from JEITA CP-6101B, Table B-2, with permission from JEITA.			

B.5.3 Decoder

The serial data S that comes from the RX front-end is converted as shown in Figure B.7, Figure B.8, Table B.5 and Table B.6.

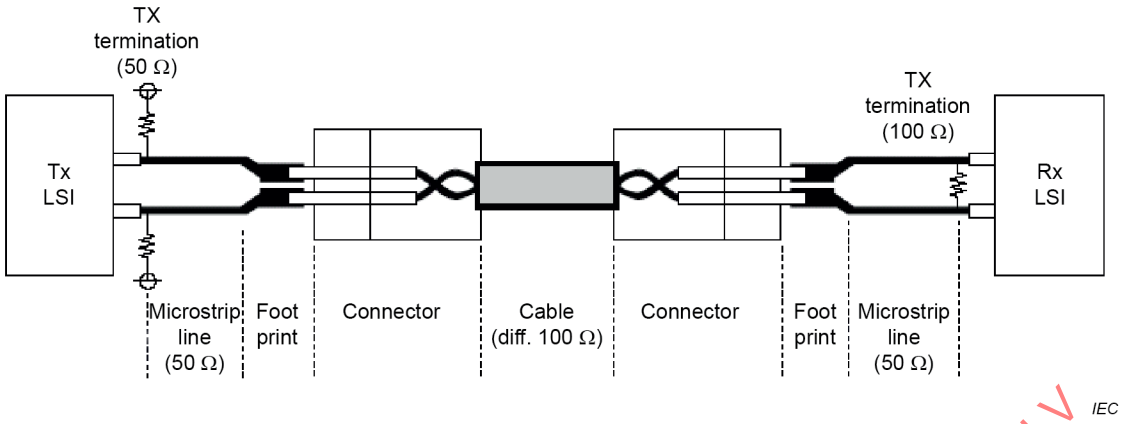
B.6 Transmission system and transmission line of electrical characteristics

The transmission systems (see Figure B.9) are required to meet the specifications below.

- The differential impedance shall meet the specification stated in Figure B.10. A transmission line has a small and gradual attenuation.
- A transmission line loss on a cable shall be less than −15 dB at 1 GHz in accordance with $\sqrt{f}$ attenuation (see Figure B.11).

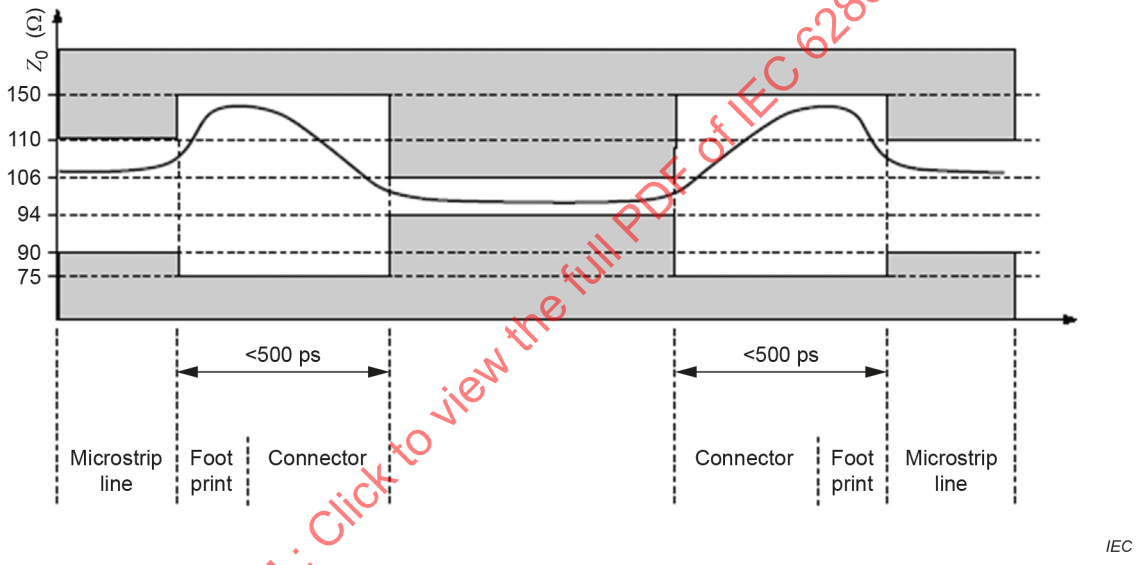
The differential signal cable skew time shall be:

- less than 30 % of one bit time (SFTCLK > 33 MHz);
- less than 24 % of one bit time (SFTCLK ≤ 33 MHz).



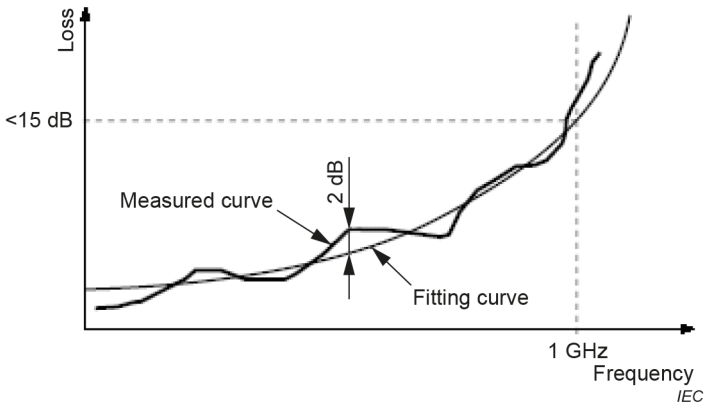
Reproduced from JEITA CP-6101B, Figure 9-1, with permission from JEITA.

Figure B.9 – Transmission system



Reproduced from JEITA CP-6101B, Figure 9-2, with permission from JEITA.

Figure B.10 – Transmission line tolerance impedance



Reproduced from JEITA CP-6101B, Figure 9-3, with permission from JEITA.

Figure B.11 – Transmission loss

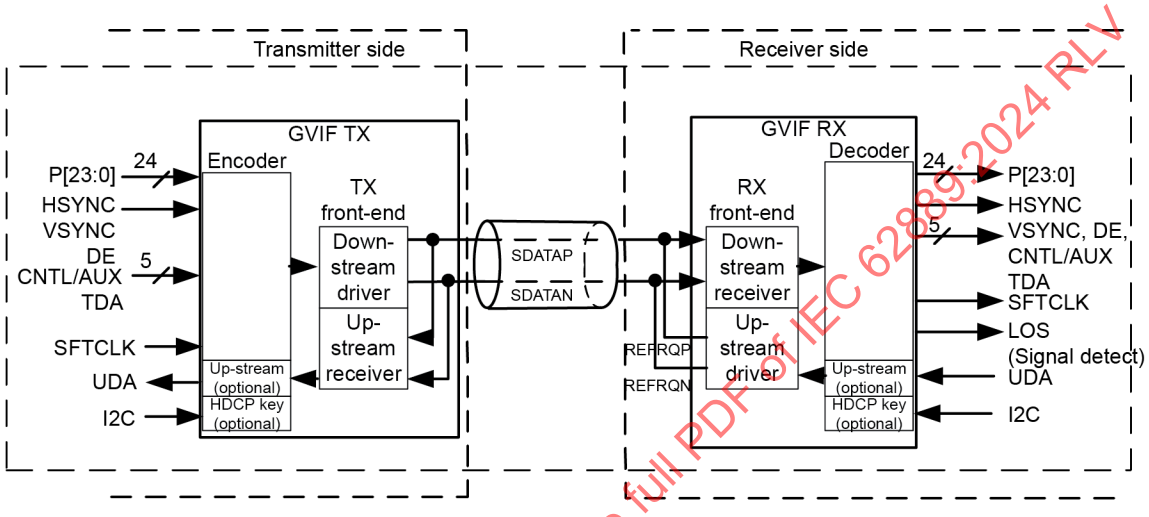
~~Annex A~~Annex C
(informative)

GVIF Multiple link application

C.1 Single-link application example

C.1.1 Block diagram for single-link transmission

A block diagram of a differential single link is shown in Figure C.1.



Reproduced, with modifications, from JEITA CP-6101B, Figure 3-1, with permission from JEITA.

Figure C.1 – Differential single-link block diagram

The downstream transmission signal is the encoded serial P[23:0], HSYNC, VSYNC, DE, CNTL/AUX, SDA and TDA 30-bit data by the GVIF TX encoder. These data are in all of the SFTCLK domains, and they can be regenerated by the GVIF RX decoder. The encoder and decoder perform in accordance with Clause B.5.

The LOS signal output on the receiver side is asserted when GVIF RX receives no differential signal input or the clock and data recovery circuit in GVIF RX does not generate recovered SFTCLK (loss of lock).

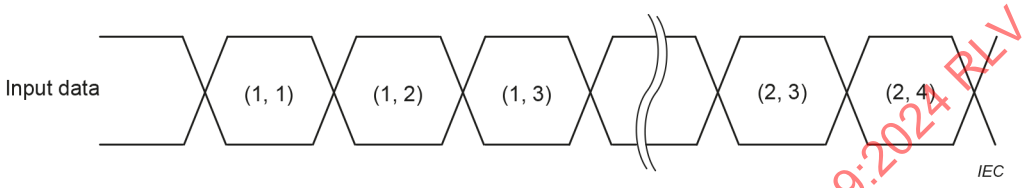
There are optional functions for downstream and upstream user-defined signal transmissions with the terminal names CNTL/AUX and TDA for downstream and UDA for upstream, as shown in Figure C.1. AUX can also optionally use an audio-enable signal.

Additionally, HDCP (high-bandwidth digital contents protection) is also defined as an optional function. The I2C inputs for both GVIF TX and GVIF RX are input terminals to control the HDCP authentication function. The SDA (optional) is generated by an I2C signal order, i.e. a signal to exchange a HDCP key between GVIF TX and GVIF RX.

C.1.2 Data mapping of single-link transmission

A data mapping array should be assigned pixel data of an LCD module, as shown in Figure C.2.

(1,1)	(1,2)	(1,3)	(1,4)	
(2,1)	(2,2)	(2,3)	(2,4)	
(3,1)	(3,2)	(3,3)	(3,4)	
(4,1)	(4,2)	(4,3)	(4,4)	



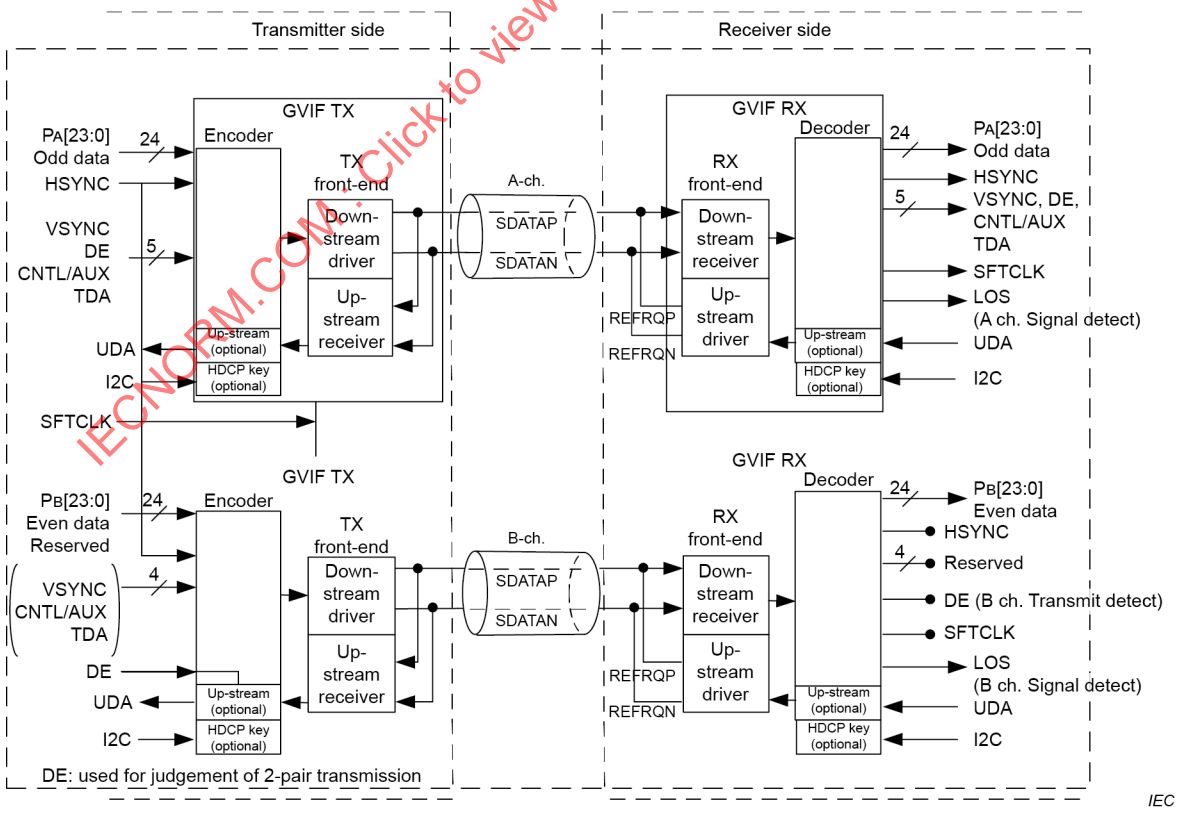
Reproduced from JEITA CP-6101B, Figure 8-1, with permission from JEITA.

Figure C.2 – Pixel configuration

C.2 Multiple-link application example

C.2.1 Block diagram for 2-pair parallel transmission

A block diagram of a multiple-link system configuration is shown in Figure C.3. Each channel is called A-channel and B-channel.



Reproduced, with modifications, from JEITA CP-6101B, Figure 3-1, with permission from JEITA.

Figure C.3 – Multiple-link application block diagram

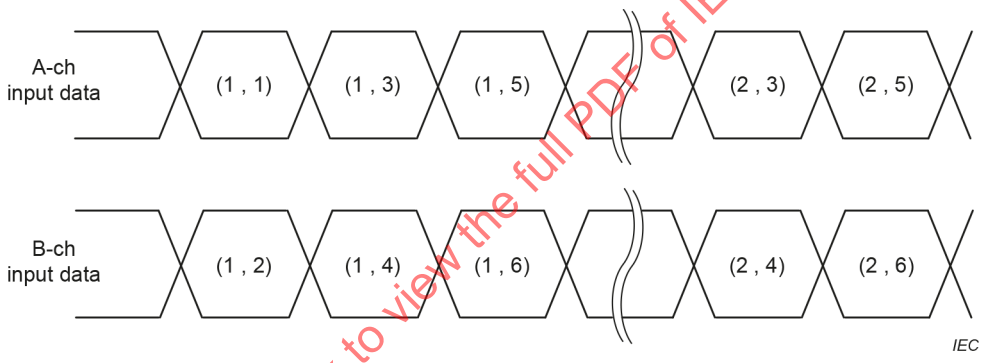
In order to switch between a 1-pair transmission system and 2-pair transmission system, a detection circuit is necessary on the transmitter side. In the case of a 2-pair transmission system, the DE equivalent signal is input to the "DE" pin of the B-ch, and in the case of a 1-pair transmission system, the fixed signal is input to the "DE" pin of the A-ch.

C.2.2 Data mapping of 2-pair transmission

Odd data should be assigned to the A-ch, even data should be assigned to the B-ch.

A data-mapping array for an LCD module is shown in Figure C.4.

(1,1)	(1,2)	(1,3)	(1,4)	
(2,1)	(2,2)	(2,3)	(2,4)	
(3,1)	(3,2)	(3,3)	(3,4)	
(4,1)	(4,2)	(4,3)	(4,4)	
A-ch. data	B-ch. Data	A-ch. data	B-ch. data	



Reproduced from JEITA CP-6101B, Figure 8-2, with permission from JEITA.

Figure C.4 – Pixel configuration when using 2-pairs

Bibliography

IEC 62315-1:2003, *DTV profiles for uncompressed digital video interfaces – Part 1: General*

JEITA CP-6101B, Digital monitor interface GVIF, available at *https://www.jeita.or.jp/japanese/standard/book/CP-6101B_J/*

ARIB (Association of Radio Industries and Businesses) STD-B21, *Receiver for Digital Broadcasting (Desirable Specifications)*

ARIB (Association of Radio Industries and Businesses) TR-B14, *Operational Guidelines for Digital Terrestrial Television Broadcasting*

Digital Content Protection LLC, available at http://www.digital-cp.com/

ANSI/TIA/EIA-644-1995, *Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits*, November 1995

I2C-bus specification and user manual Rev. 7.0 –1 October 2021, available at https://www.nxp.com/docs/en/user-guide/UM10204.pdf

IEC 62889

Edition 2.0 2024-02

INTERNATIONAL STANDARD

NORME INTERNATIONALE

colour inside

Digital video interface – Gigabit video interface for multimedia systems

Interface vidéo numérique – Interface vidéo gigabit pour les systèmes multimédias

IEC 62889:2024-02(en-fr)

CONTENTS

INTERNATIONAL ELECTROTECHNICAL COMMISSION

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DIGITAL VIDEO INTERFACE – GIGABIT VIDEO INTERFACE FOR MULTIMEDIA SYSTEMS

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JEITA CP-6101B served as a basis for the elaboration of this document.

This second edition cancels and replaces the first edition published in 2015. This edition constitutes a technical revision.

This edition includes the following significant technical changes with respect to the previous edition:

a) Addition of a new technology interface, GVIF2.

The text of this International Standard is based on the following documents:

Draft	Report on voting
100/3912/CDV	100/4040/RVC

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/publications.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under webstore.iec.ch in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn, or
- revised.

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INTRODUCTION

This International Standard is based on JEITA CP-6101B: *Digital monitor interface GVIF*, which was originally specified by the Japan Electronics and Information Technology Industries Association (JEITA).

The Gigabit Video InterFace (GVIF) is a serial point-to-point interface supporting uncompressed digital video links that was designed to address the needs of automotive navigation and entertainment systems, etc., to transport baseband digital video information. GVIF applies low-voltage differential signalling (LVDS) technology and makes use of a thin cable consisting of a single shielded twisted pair of conductors that exhibits high noise immunity and low EMI, and is optimized for small size and low weight. GVIF supports display resolutions ranging from WQVGA through WUXGA with a maximum of 24 bits per pixel colour video data, and can transmit a baseband video signal over cable lengths over 10 m. Optionally, GVIF supports audio data transmission and user data transmission.

Gigabit Video InterFace 2(GVIF2) is a baseband transmission method for digital video information that applies serial data transmission technology. In the downstream transmission from GVIF2 TX to GVIF2 RX, the high-bandwidth data for video information (GHDS) and the device control signal (GLDS) are transmitted by using the time-division multiplexing method. In the upstream transmission from GVIF2 RX to GVIF2 TX, the control signal GLUS is transmitted. The upstream transmission and downstream transmission occur in full duplex. Optionally, GVIF2 also supports audio data transmission and user data transmission.

Also optionally, when paired with high-bandwidth digital content protection (HDCP), the GVIF's standard functions and features address all of the requirements for delivering content-protected video from a source to a video display monitor.

This document describes the GVIF family that consists of GVIF2 in the main body and Annex A, and GVIF in Annex B and Annex C.

GVIF2 has the following features:

- transmission by a differential shielded twisted-pair cable or coaxial cable,
- to enable multiple video and audio content transmission using time-division multiplexing,
- possibility to use audio transmission, bi-direction user communication, and HDCP (high-bandwidth digital content protection) technology (optional),
- availability for daisy chain transmission (optional).

The Association of Radio Industries and Businesses (ARIB) refers to GVIF and GVIF2 in its standard ARIB STD-B21 as being authorized digital video output interfaces.

DIGITAL VIDEO INTERFACE – GIGABIT VIDEO INTERFACE FOR MULTIMEDIA SYSTEMS

1 Scope

This document describes two serial digital interfaces, Gigabit Video InterFace (GVIF) and Gigabit Video InterFace2 (GVIF2), for the interconnection of digital video equipment. GVIF and GVIF2 are primarily intended to carry high-speed digital video data for general usage and are well suited for multimedia entertainment systems in a vehicle.

This document specifies the physical layer of the interface, including transmission line characteristics and electrical characteristics of transmitters and receivers. Mechanical and physical specifications of connectors are not included.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

ITU-R BT.601-5, *Studio encoding parameters of digital television for standard 4:3 and wide-screen 16:9 aspect ratios*

ITU-R BT.656-5, *Interface for digital component video signals in 525-line and 625-line television systems operating at the 4:2:2 level of Recommendation ITU-R BT.601*

3 Terms, definitions and abbreviated terms

3.1 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminology databases for use in standardization at the following addresses:

- IEC Electropedia: available at https://www.electropedia.org/
- ISO Online browsing platform: available at https://www.iso.org/obp

3.1.1
DE
display enable signal given in IEC 62315-1

3.1.2
HSYNC
display horizontal synchronous signal given in IEC 62315-1

3.1.3
VSYNC
display vertical synchronous signal given in IEC 62315-1

3.1.4
RGB
display red, green, blue colour data input (TX) or output (RX) given in ITU-R BT.601-5 and ITU-R BT.656-5

3.1.5
CNTL/AUX
downstream user-defined signal or audio enable signal

3.1.6
P[23:0]
digital signal data such as 24-bit colour video data, for example RGB data input (TX) or output (RX)

3.1.7
GHDS
GVIF2 High bandwidth DownStream
high-bandwidth downstream content data of the GVIF2 format

3.1.8
GLDS
GVIF2 Low bandwidth DownStream
low-bandwidth downstream control signal data of the GVIF2 format

3.1.9
GLUS
GVIF2 Low bandwidth UpStream
low-bandwidth upstream control signal data of the GVIF2 format

3.1.10
GVIF RX
circuit that receives the serial signal from a shielded-pair transmission line, decodes it and converts it into a parallel video signal

3.1.11
GVIF TX
circuit that receives the parallel video signal and the control signals, and encodes them into serial data to send a signal by driving a shielded-pair transmission line

3.1.12
GVIF2 RX
circuit that receives the serial signal from a shielded twisted-pair cable or coaxial cable, decodes it and converts it into video and audio/control signals

3.1.13
GVIF2 TX
circuit that receives the video and audio/control signals, encodes them into serial data and sends a signal by driving a shielded twisted-pair cable or coaxial cable

3.1.14
LOS
loss of signal detection, asserted when the differential input signal at the receiver cannot be received

3.1.15
RX front-end
front-end block of receiver side

3.1.16
SDA
serial data down-stream signal

3.1.17
SDATA
GVIF2 serial data signal on coaxial cable transmission

3.1.18
SDATAP
down-stream positive-phase side signal of the differential serial data

3.1.19
SDATAN
down-stream negative-phase side signal of the differential serial data

3.1.20
REF
reference signal

3.1.21
REFRQP
current source positive signal for reference clock request from RX side

3.1.22
REFRQN
current source negative signal for reference clock request from RX side

3.1.23
SFTCLK
pixel clock for capture of the parallel video data per pixel

3.1.24
TDA
transmit data down-stream user-defined signal

3.1.25
TX front-end
front-end block of transmitter side

3.1.26
UDA
up-stream user defined ancillary data signal

3.1.27
IRQ
up-stream common-mode reference request current for REFRQP/N

3.1.28
VOS
common-mode voltage amplitude of reference request

3.1.29
VOD
differential voltage amplitude for SDATAP/N

3.1.30
VDD
power supply on the transmitter side

3.1.31
V_SDATAP
single-ended voltage of SDATAP

3.1.32
V_SDATAN
single-ended voltage of SDATAN

3.1.33
TP1
test point of a downstream eye mask specification

3.1.34
TP2
test point of an upstream eye mask specification

3.1.35
normalized differential voltage
voltage of transmitter output point

3.1.36
UI
normalized time unit interval of transmitter output point

3.1.37
WSYNC
word synchronized signal

3.2 Abbreviated terms

AC	alternating current
DC	direct current
EMI	electro-magnetic interference
GVIF	Gigabit Video InterFace
HDCP	high-bandwidth digital content protection
LSB	least significant bit
LVDS	low voltage differential signalling
MSB	most significant bit
PRBS	pseudo random binary sequence

4 Architecture

The GVIF2 has a higher capability multimedia interface and is considered as the next generation of GVIF, which is described in Annex B and Annex C.

The GVIF2 transmission line is a shielded twisted-pair cable with the differential characteristic impedance Z0_diff or a coaxial cable with the characteristic impedance Z0_coax, and is connected to GVIF2 RX and GVIF2 TX, with an AC coupling capacitor, and high-frequency terminated resistor (see Figure 1). The signal path of the transmission line of GVIF2 is DC isolated from both GVIF2 TX and GVIF2 RX. The shield of the transmission line of GVIF2 is connected to the GND of the TX circuit and of the RX circuit.

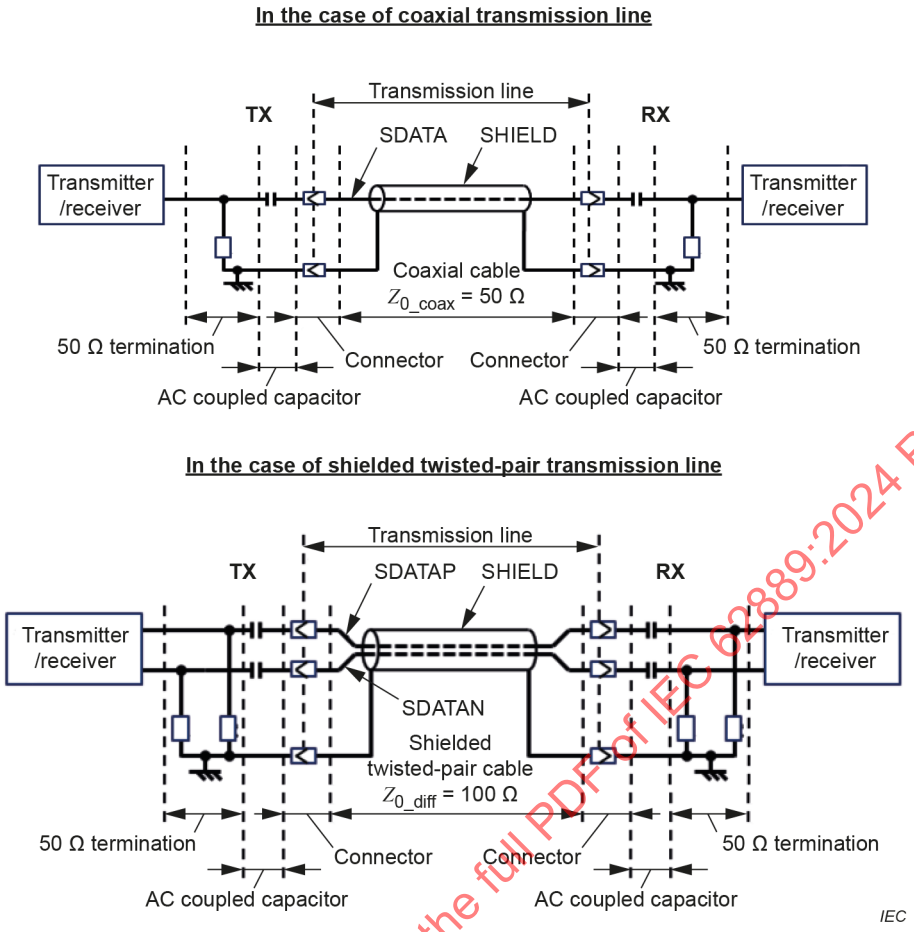

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Figure 1 – Architecture of the GVIF2

5 Electrical characteristics

5.1 General

AC specifications described in below shall be satisfied. GVIF2 does not specify DC specifications because the transmission architecture of GVIF2 is a complete AC coupling.

5.2 AC electrical specifications

The AC electrical specifications of the transmitter and receiver side are given in Table 1. The definition of voltage levels are shown in Figure 2, and Figure 3 and Figure 4 show a downstream eye mask specification at TP1 and an upstream eye mask specification at TP2 for GVIF2.

Table 1 – AC electrical specification of GVIF2

	Downstream bit rate			Upstream bit rate
	Fdownstream_1	Fdownstream_2	Fdownstream_3	Fupstream
	Gbit/s	Gbit/s	Gbit/s	Mbit/s
Minimum	2,16	3,24	4,32	9,0
Maximum	2,4	3,6	4,8	10,0
Fupstream = Fdownstream_1/240 or Fupstream = Fdownstream_2/360 or Fupstream = Fdownstream_3/480				
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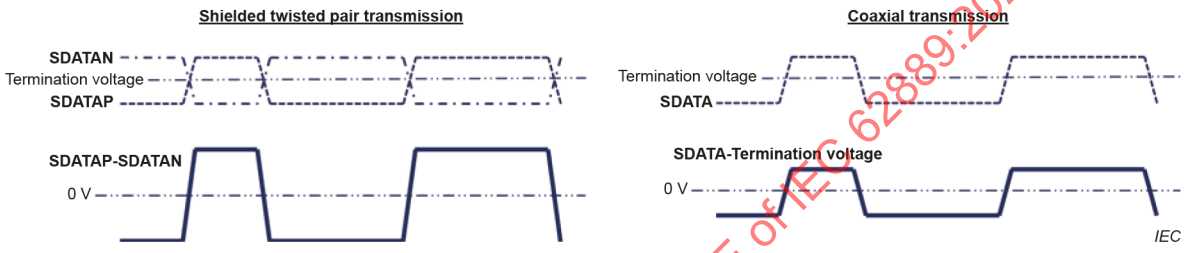

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Figure 2 – Level definition of GVIF2

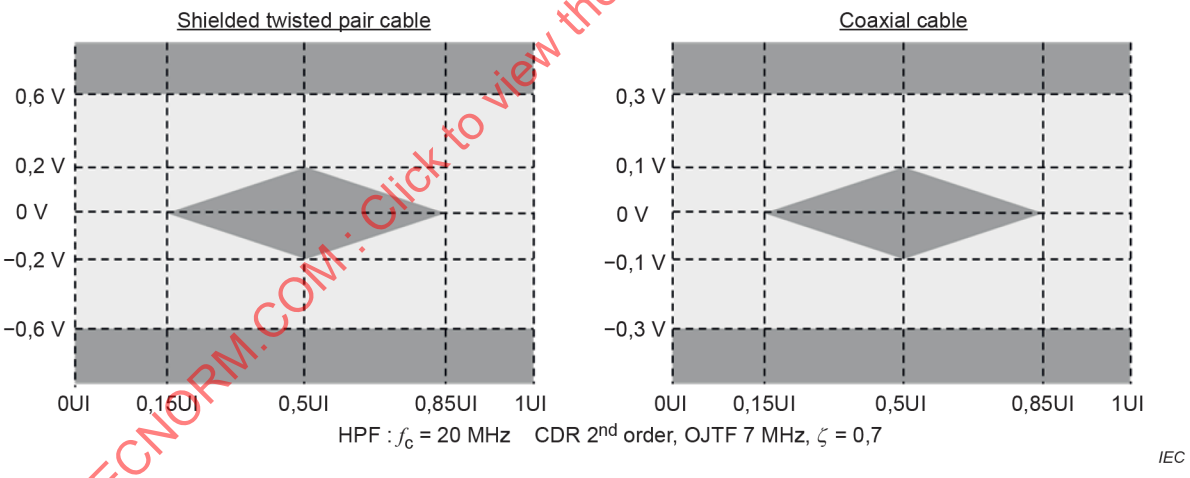

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Figure 3 – GVIF2 downstream eye mask (at TP1)

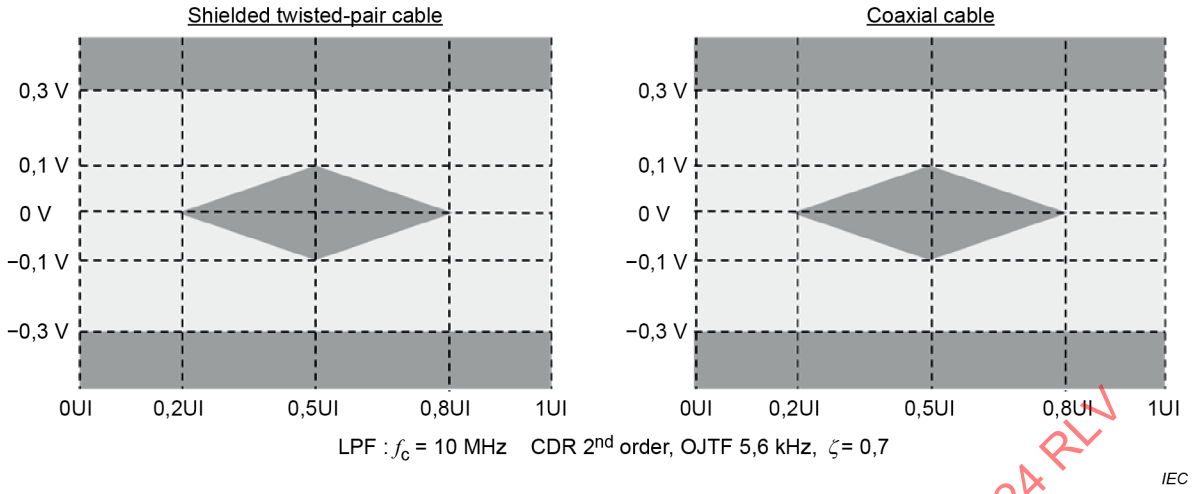

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Figure 4 – GVIF2 upstream eye mask (at TP2)

6 Front-end

6.1.1 General

The front-end block diagram of GVIF2 is shown in Figure 5.

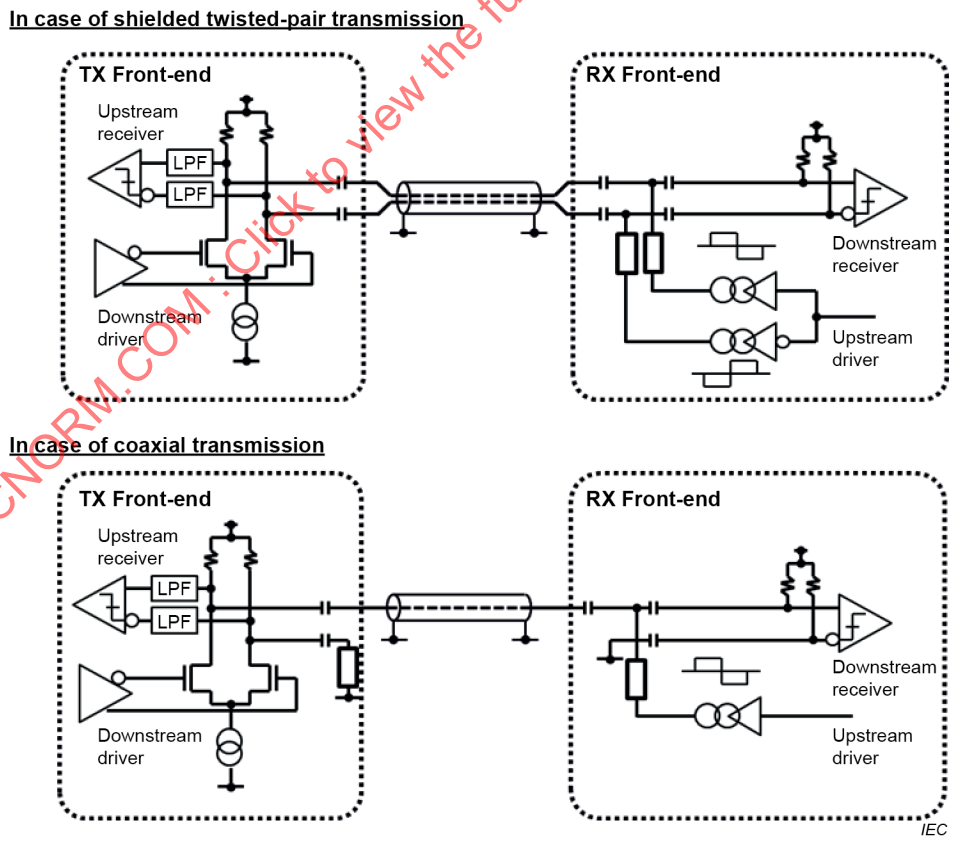

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Figure 5 – Front-end block diagram of GVIF2

6.1.2 TX Front-end

The GVIF2 TX front end consists of AC coupling capacitors, termination resistors, a downstream driver, an upstream receiver, and connectors. The termination resistors, as the load of the differential current from the downstream driver, generate the downstream signal voltage, and become the high-frequency termination of the transmission line. The upstream receiver reproduces the data extracted by the low-pass filter (LPF) from the upstream signal transmitted by the RX.

6.1.3 RX Front-end

The GVIF2 RX front end consists of AC coupling capacitors, termination resistors, a downstream receiver and an upstream driver. The downstream receiver reproduces the data from the downstream signal which is transmitted from the TX and extracted by the high-pass filter (HPF), which consists of the AC coupling capacitors and the termination resistors. The upstream driver drives the upstream signal to the transmission line via the LPF. The upstream signal is in frequency synchronization with the downstream signal, and the transmitted rate is 10 Mbit/s at maximum, which is proportional to the downstream rate.

6.1.4 Configuration block diagram

Downstream signal is GHDS and GLDS encoded in the downstream code, and the transmission rate shall be selected from 2,4 Gbit/s, 3,6 Gbit/s, or 4,8 Gbit/s according to the bandwidth required for GHDS.

GHDS shall be set by a time-division multiplexing in DATA SLOT units.

GHDS may use multiple video (and audio) contents transmission (optional, see Annex A).

Upstream signal shall be GLUS-encoded in upstream code.

Upstream and downstream shall be transmitted simultaneously (full duplex) by frequency division.

The GVIF2 configuration block diagram data mapping is shown in Figure 6.

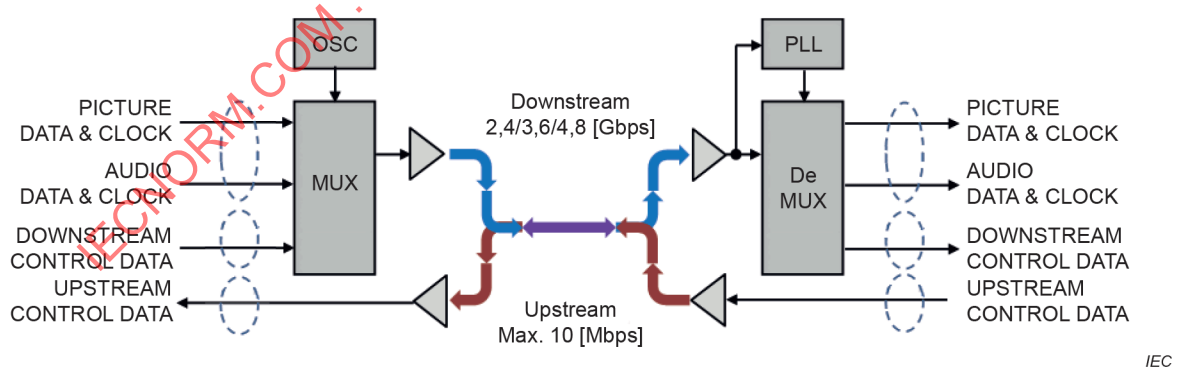

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Figure 6 – GVIF2 configuration block diagram Data mapping

6.1.5 Data mapping

6.1.5.1 RGB888 data mapping for GHDS

RGB888 data and synchronization signals VSYNC/HSYNC/DE shall be mapped into GHDS as shown in Figure 7.

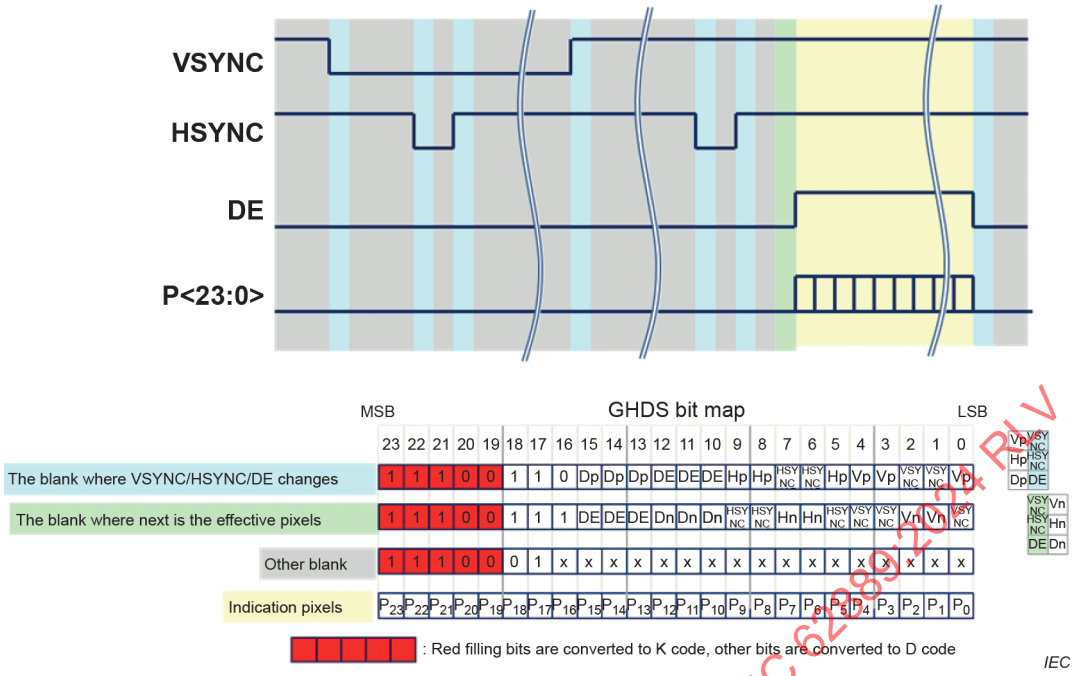

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Figure 7 – GVIF2 RGB888 data mapping

6.1.5.2 Mapping of content for other formats (optional)

MAINDATA, MAINCTRL, SUBDATA can be mapped into GHDS following the agreement of coordination between GVIF2 TX and GVIF2 RX, as shown in Figure 8. It is recommended that video pixel data be mapped into MAINDATA, video synchronization signals be mapped into MAINCTRL, and audio signals (optional) be mapped into SUBDATA.

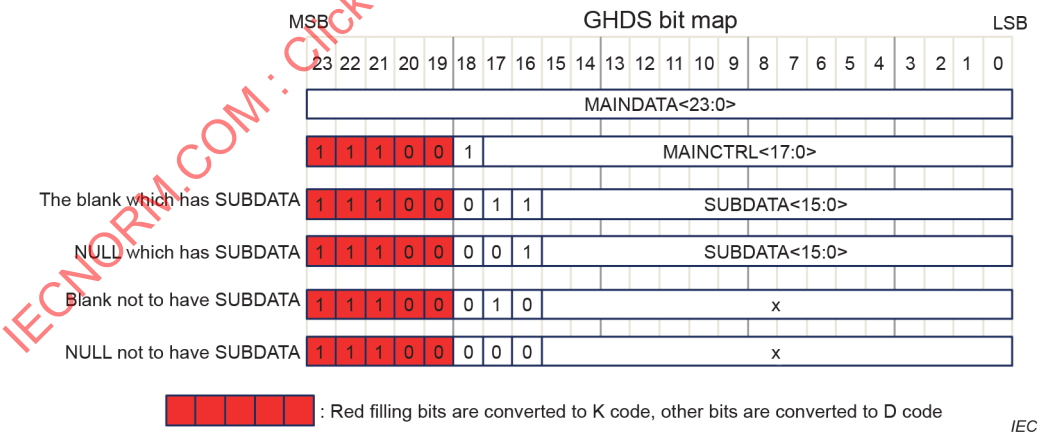

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Figure 8 – GVIF2 mapping for general content data(optional)

Bi-directional communication signals between GVIF2 TX and GVIF2 RX, such as UART, can be mapped into GLDS and GLUS (optional).

Certification data for HDMI (HDCP) is recommended to be mapped into SUBDATA, GLDS, GLUS, and a part of GHDS (optional).

7 Transition state link

The transition state diagram of GVIF2 TX and GVIF2 RX is shown in Figure 9.

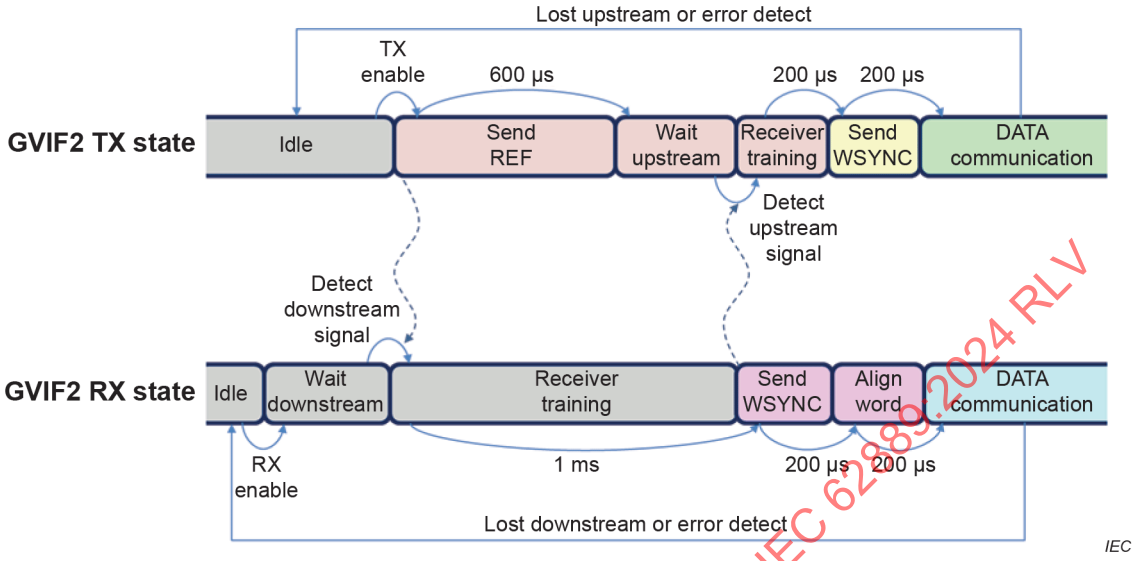

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Figure 9 – Transaction state diagram of GVIF2

In the GVIF2 TX connected to the GVIF2 RX, there are several states including a state without down-stream signal (Idle), states transmitting a REF signal (Send REF, Wait Upstream, Receiver Training), a state transmitting a SYNC signal (Send WSYNC), and a normal downstream transmission state. While it shall transit from Idle to Send REF when the TX circuit is activated, and shall transit from Wait Upstream to Receiver Training when the upstream signal is detected, the other transitions shall occur unconditionally in the specified time. If the upstream signal is not detected in the normal downstream transmission state or an error is detected in the upstream signal, it shall transit to Idle.

In the GVIF2 RX connected to the GVIF2 TX, there are several states, including a state without upstream signal (Idle, Wait Downstream, Receiver Training), states transmitting a SYNC signal (Send WSYNC, Align Word), and a normal upstream transmission state. While it shall transit from Idle to Waite Downstream when the RX circuit is activated, and shall transit from Wait Downstream to Receiver Training when the down-stream signal is detected, the other transitions shall occur unconditionally in the specified time. If the downstream signal is not detected in the normal upstream transmission state, or an error is detected in the down-stream signal, it shall transit to Idle.

The downstream REF and WSYNC signals output from the GVIF2 TX shall be the encoded GHDS and GLDS (see Figure 10).

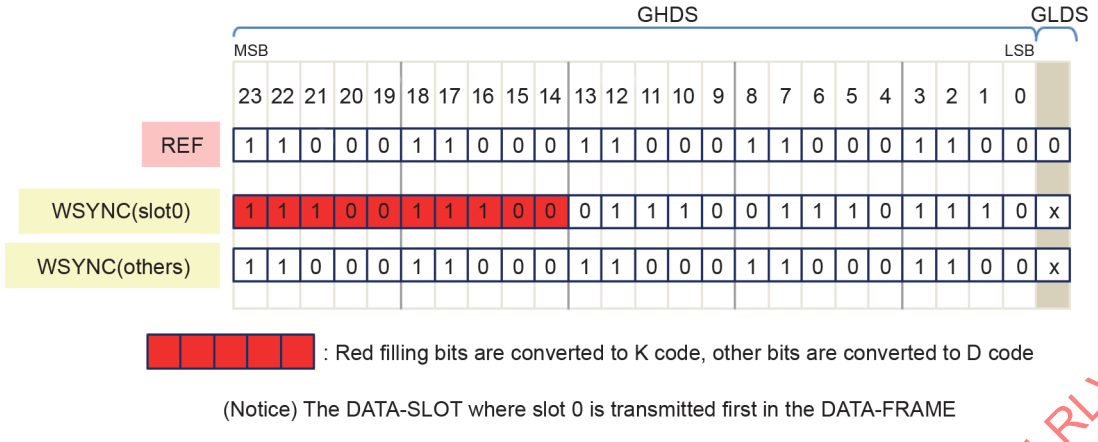

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Figure 10 – REF and WSYNC signals of GVIF2 downstream

The upstream WSYNC signal output from GVIF2-RX shall be the encoded GLUS in Figure 11.

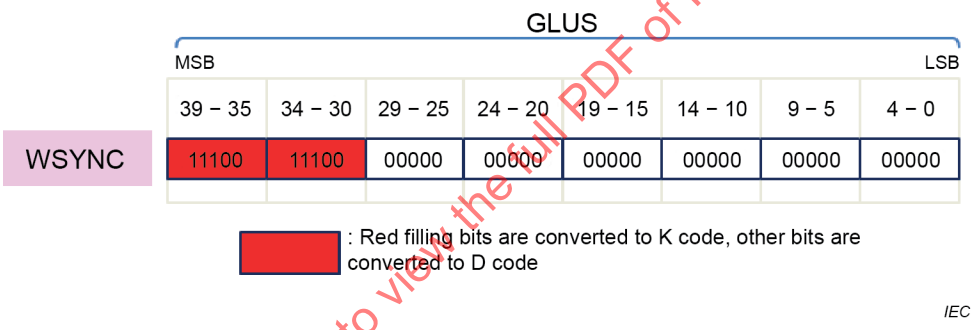

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Figure 11 – WSYNC signal of upstream

8 Protocol

8.1 Downstream encoder

8.1.1 General

The downstream encoder shall perform operations of GHDS and GLDS concatenation, scrambling, and the 5B/6B conversion shown in Figure 12.

8.1.2 GHDS and GLDS concatenation

The 25-bit word shall be generated with 24-bit GHDS on the MSB side and 1-bit GLDS on the LSB side.

8.1.3 Scrambler

The part of word column which is converted to D code shall be scrambled by PRBS31 (pseudorandom binary sequence 31).

8.1.4 5B/6B conversion

The 25-bit word shall be divided into 5 bits and each 5-bit data shall be converted to the 6-bit D code or K code in accordance with Table 2. The generated 30-bit downstream data shall be converted to serial data and shall be transmitted to the RX leading with the MSB.

Table 2 – 5B/6B conversion

Input		RD = −1	RD = +1		Input		RD = −1	RD = +1
Code	EDCBA	abcdei			Code	EDCBA	abcdei	
D.00	00000	100111	011000		D.16	10000	011011	100100
D.01	00001	011101	100010		D.17	10001	100011	
D.02	00010	101101	010010		D.18	10010	010011	
D.03	00011	110001			D.19	10011	110010	
D.04	00100	110101	001010		D.20	10100	001011	
D.05	00101	101001			D.21	10101	101010	
D.06	00110	011001			D.22	10110	011010	
D.07	00111	111000	000111		D.23	10111	111010	000101
D.08	01000	111001	000110		D.24	11000	110011	001100
D.09	01001	100101			D.25	11001	100110	
D.10	01010	010101			D.26	11010	010110	
D.11	01011	110100			D.27	11011	110110	001001
D.12	01100	001101			D.28	11100	001110	
D.13	01101	101100			D.29	11101	101110	010001
D.14	01110	011100			D.30	11110	011110	100001
D.15	01111	010111	101000		D.31	11111	101011	010100
					K.28	11100	001111	110000
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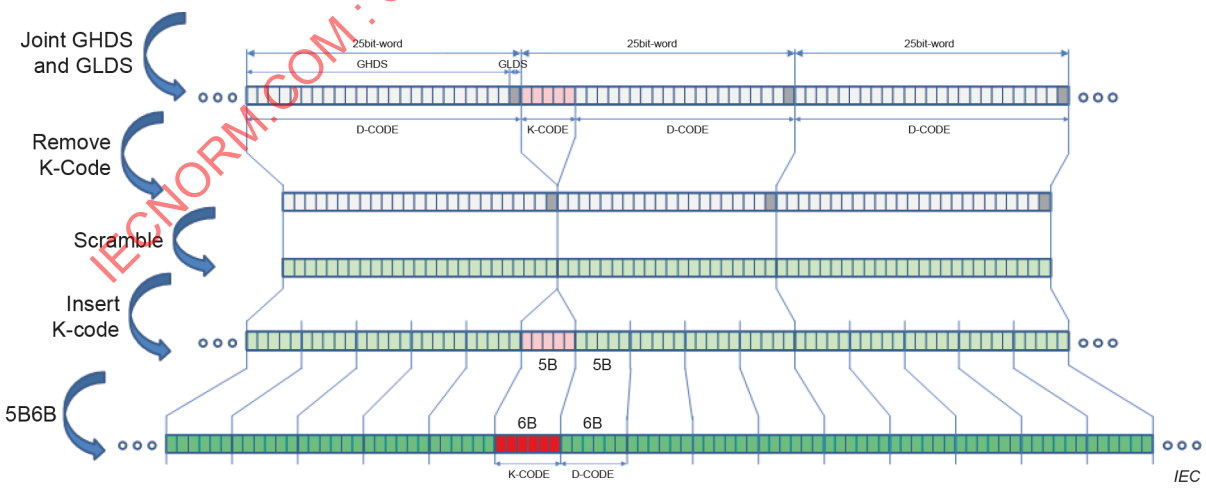

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Figure 12 – Downstream encoding

8.2 Downstream decoder

The decoder shall perform reverse operation of the downstream encoder, that is 6-bit to 5-bit reverse conversion, descrambling, and GHDS/GLDS decomposition, as shown in Figure 13.

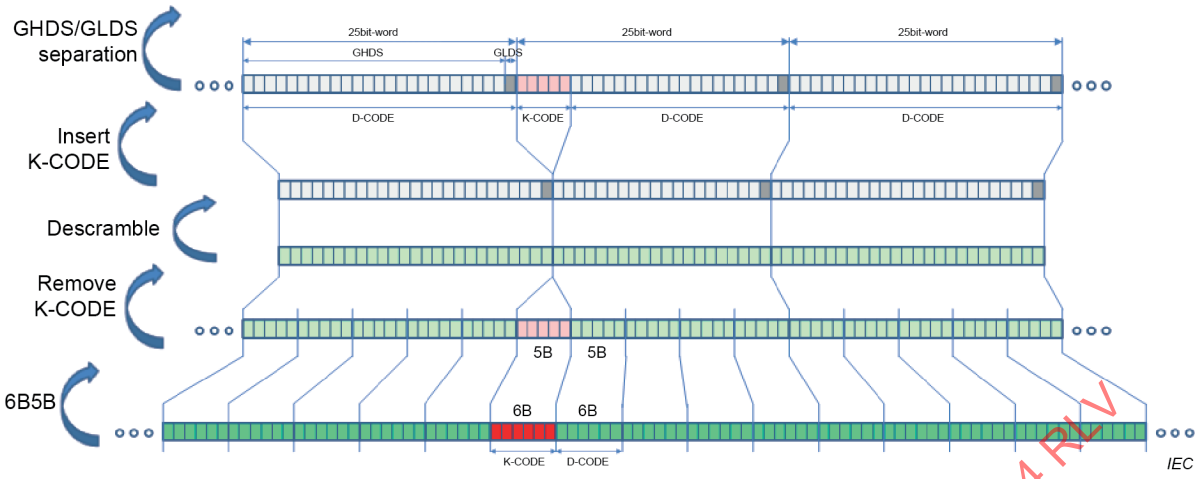

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Figure 13 – Downstream decoding

8.3 Upstream encoder

8.3.1 GLUS concatenation

GLUS data includes 4-bit length GLUS0, updated 8 times, 1-bit length GLUS1 and GLUS2, updated twice, and 1-bit length GLUS3, GLUS4, GLUS5 and CHK (checksum), updated once, for every 4,8 µs. The GLUS data shall be compiled as shown in the Figure 14 to generate a 40-bit GLUS word.

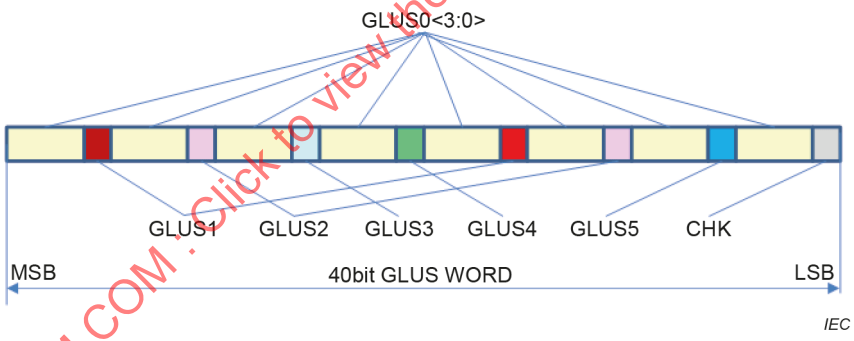

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Figure 14 – GLUS word structure

8.3.2 Scrambler

The part of word column which is converted to D code shall be scrambled by PRBS7 (pseudorandom binary sequence 7).

8.3.3 5B/6B conversion

The 40-bit word is divided into 5 bits and each 5-bit data is converted into the 6-bit D code, in accordance with Table 2. The generated 48-bit length upstream data is converted to serial data and shall be transmitted to GVIF2 TX, with a leading MSB.

8.3.4 Upstream decoder

The decoder shall perform the reverse operation of the upstream encoder, which is 6-bit to 5-bit reverse conversion, descrambling, and decomposition into GLUS 0 to 5.

9 Transmission system and transmission line of electrical characteristics

The transmission line characteristics of GVIF2 are defined by the TP1 and TP2 (test points) in Figure 15.

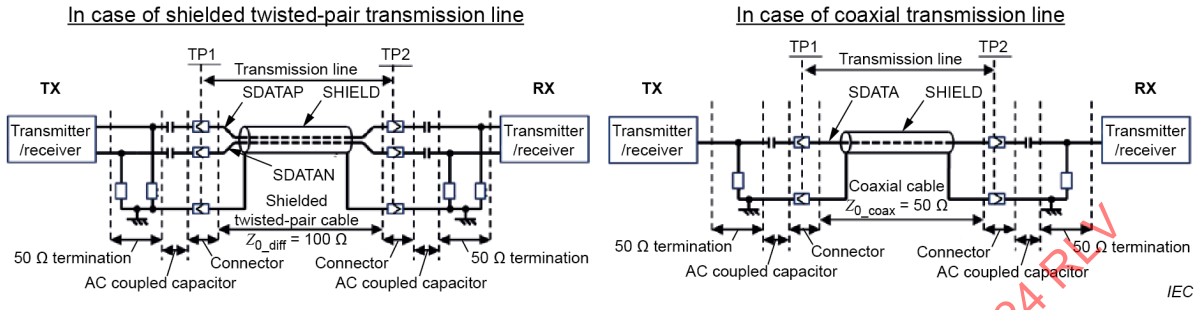

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Figure 15 – Test points of GVIF2

The shielded twisted-pair cable and coaxial cable (TP1 to TP2) should meet the S21 template in Figure 16.

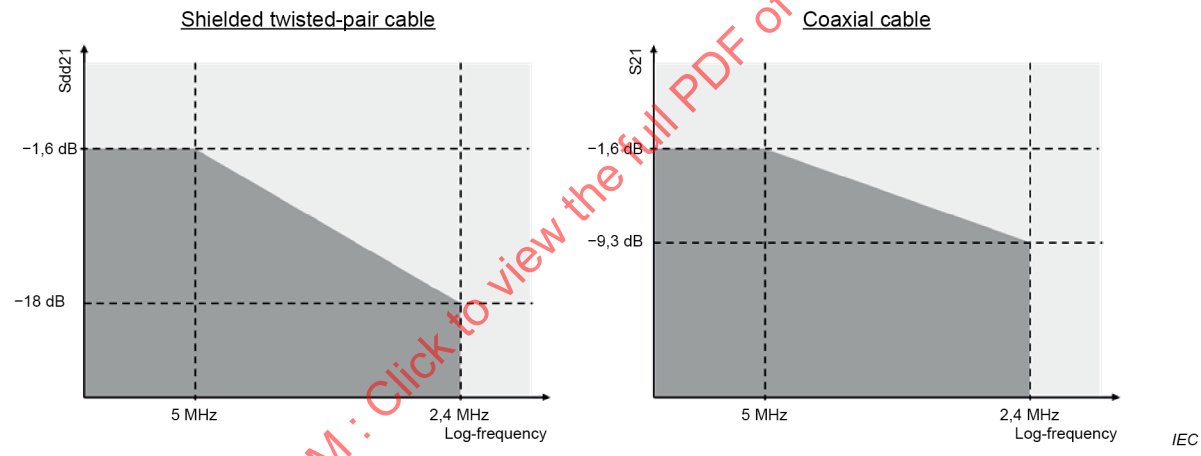

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Figure 16 – S21 template for GVIF2 transmission line

Annex A
(informative)

GVIF2 multiple contents transmission

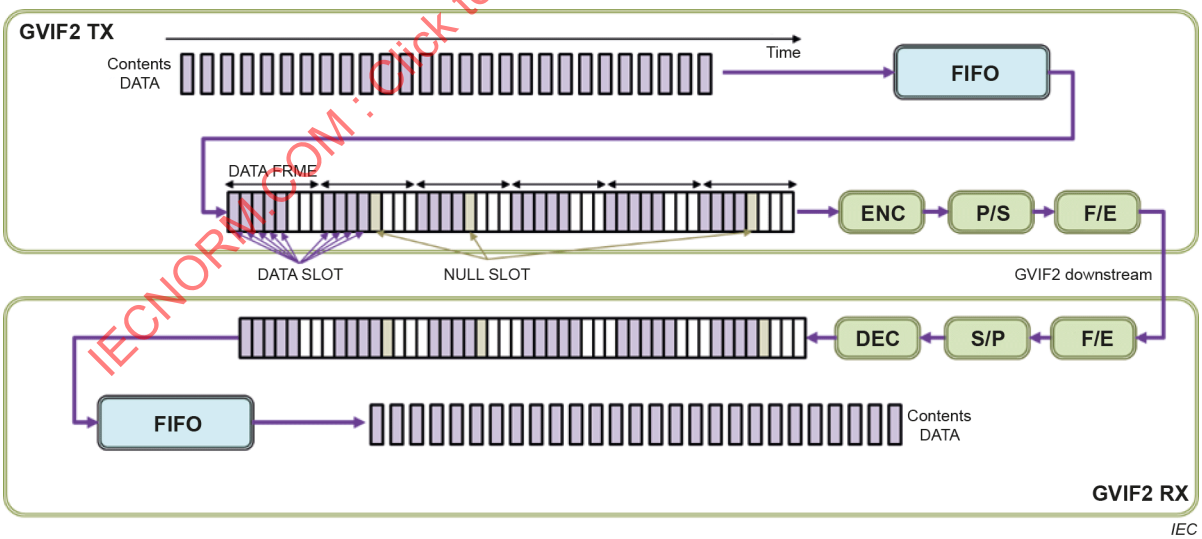
The GVIF2 downstream signal is in the unit of DATA FRAME, and the DATA FRAME has the number of DATA SLOTs specified in Table A.1. The DATA SLOT is one word (24 bits) of GHDS, in which video (and audio: optional) contents are mapped.

Data of different contents can be mapped to each DATA SLOT. In GVIF2 TX, each content is assigned the required number (fixed number) of DATA SLOTs to each DATA FRAME according to its content data bandwidth. Content data is packed into a DATA SLOT through data FIFO, but if the data FIFO is empty, the assigned DATA SLOT is padded with NULL SLOT. In GVIF2 RX, the content to be used for display is extracted from the assigned DATA SLOT and stored in the data FIFO shown in Figure A.1 and Figure A.2.

By stacking TX and RX of GVIF2 in multiple stages, it is possible to form a daisy chain that simultaneously transmits multiple contents with a shielded twisted-pair cable or a single coaxial cable (optional).

Table A.1 – GVIF2 data rate of transmission and number of the DATA SLOT

Downstream bit rate	DATA SLOT/DATA FRAME
2,4 Gbit/s	8
3,6 Gbit/s	12
4,8 Gbit/s	16
Reproduced from JEITA CP-6101B, Table 3-1, with permission from JEITA.	



Reproduced from JEITA CP-6101B, Figure 3-5, with permission from JEITA.

Figure A.1 – GVIF2 transmission for single content

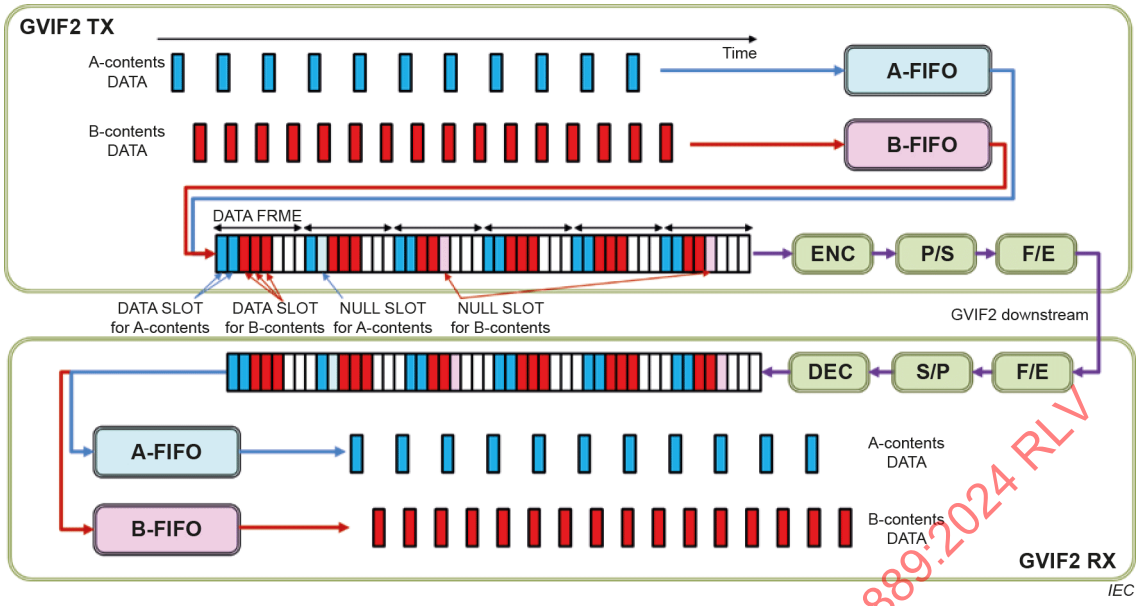


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Figure A.2 – GVIF2 multiplex transmission for multiple contents

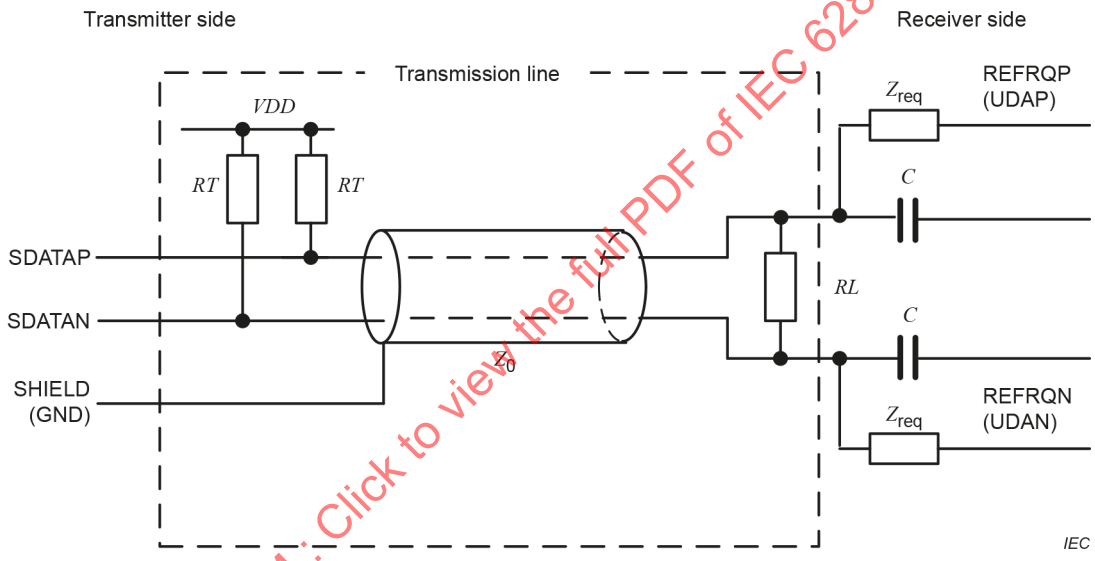
Annex B
(normative)

GVIF standard specification

B.1 Architecture

Figure B.1 illustrates the architecture of the GVIF. The fundamental operation of the GVIF is a simultaneous bi-directional data transmission technology, in which the low-voltage differential signal is transmitted down from the transmitter side to the receiver side, and the common-mode voltage signal is transmitted up from the receiver side to the transmitter side through a shielded twisted differential pair cable.

The shielded twisted-pair transmission line has the characteristic impedance Z_0 (see Figure B.1), the line is terminated to VDD by RT of (50 ± 15) Ω on the transmitter side, and is terminated carrying differential data in RL of (100 ± 5) Ω on the receiver side.



where

RT are the pull-up terminated load resistors on the transmitter side (50 ± 15) Ω;

Z_0 is the characteristic impedance of the shielded twisted-pair transmission line;

RL is the terminated resistor between differential data lines on the receiver side (100 ± 5) Ω;

C are AC coupling capacitors.

SDATAP/SDATAN are the downstream positive and negative phases side signals carrying differential serial data.

REFRQP (UDAP)/REFRQN (UDAN) is the upstream REFREQ common-mode current signal or UDA common-mode current user defined data signal. UDAP/UDAN are optional.

SHIELD (GND) is the GND and shielded ground for cable.

Z_{req} is a blocking filter for the upstream signal. It can use resistors or inductors depending on the system implementation.

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Figure B.1 – Architecture of the GVIF

B.2 Electrical characteristics

B.2.1 DC electrical specifications

The DC electrical specifications of the transmitter side are shown in Table B.1 and Figure B.2, and the DC electrical specifications of the receiver side are shown in Table B.2.

Table B.1 – DC electrical specifications of the transmitter

	VOD mV	VOS V		Input REFRQ assert current (SDATAP/N) mA	Input REFRQ de-assert current (SDATAP/N) mA
	Condition: RT = 50 Ω RL = 100 Ω	Condition: RT = 50 Ω RL = 100 Ω IRQ = 0 mA	Condition: RT = 50 Ω RL = 100 Ω IRQ = 11 mA		
Minimum	690	VDD − 0,55	VDD − 1,2		−2,0
Typical	800				
Maximum	910	VDD − 0,35	VDD − 0,8	−7,3	
Reproduced, with modifications, from JEITA CP-6101B, Table 4-1, with permission from JEITA.					

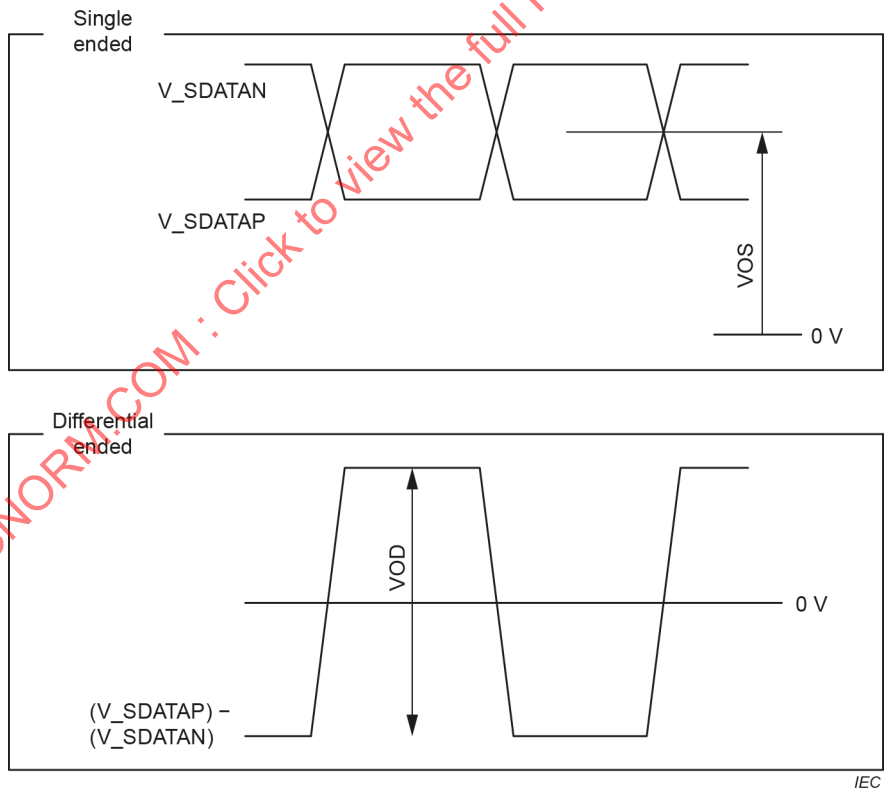

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Figure B.2 – VOD and VOS diagrams

Table B.2 – DC electrical specifications of the receiver

	Output HIGH current (REFRQP/N) mA	Output LOW current (REFRQP/N) mA
Minimum	−0,1	7,4
Maximum	0,1	11
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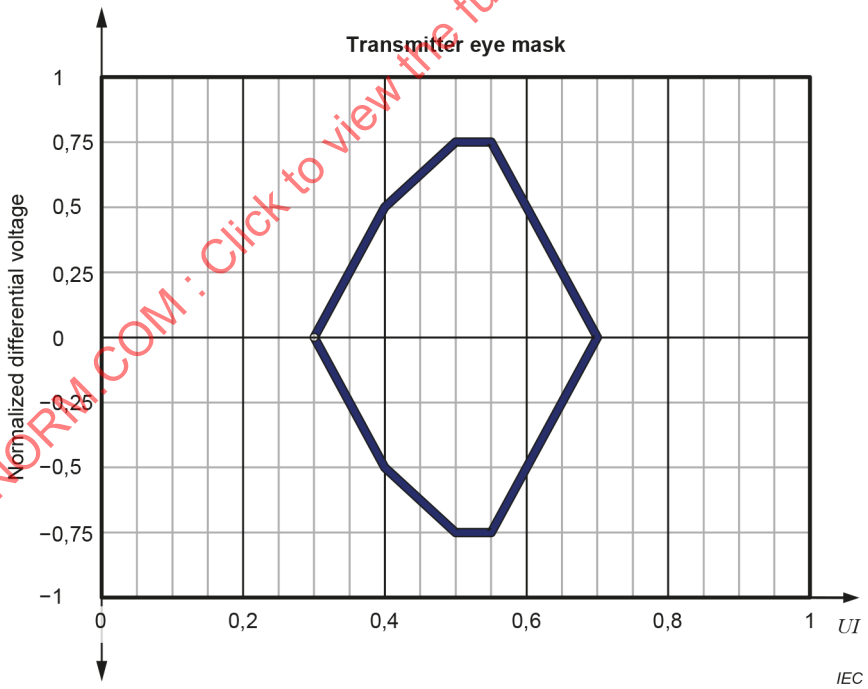
B.2.2 AC electrical specifications

The AC electrical specifications of the transmitter side are shown in Table B.3, and Figure B.3 shows a transmitter end point eye specification (TP1). The AC electrical specifications of the receiver side are shown in Table B.4.

Table B.3 – AC electrical specifications of the transmitter

	SFTCLK frequency MHz	UDA data rate (upstream) Mbit/s	SFTCLK duty factor %
Minimum	7,6	0,01	40
Maximum	160	2,41	60



Reproduced, with modifications, from JEITA CP-6101B, Figure 4-2, with permission from JEITA.

Figure B.3 – Transmitter eye mask specifications (TP1)

Table B.4 – AC electrical specifications of the receiver

	SFTCLK frequency MHz	UDA data rate (upstream) Mbit/s
Minimum	7,6	0,01
Maximum	160	2,41

B.3 Front-end

B.3.1 General

The front-end block diagram of GVIF is shown in Figure B.4.

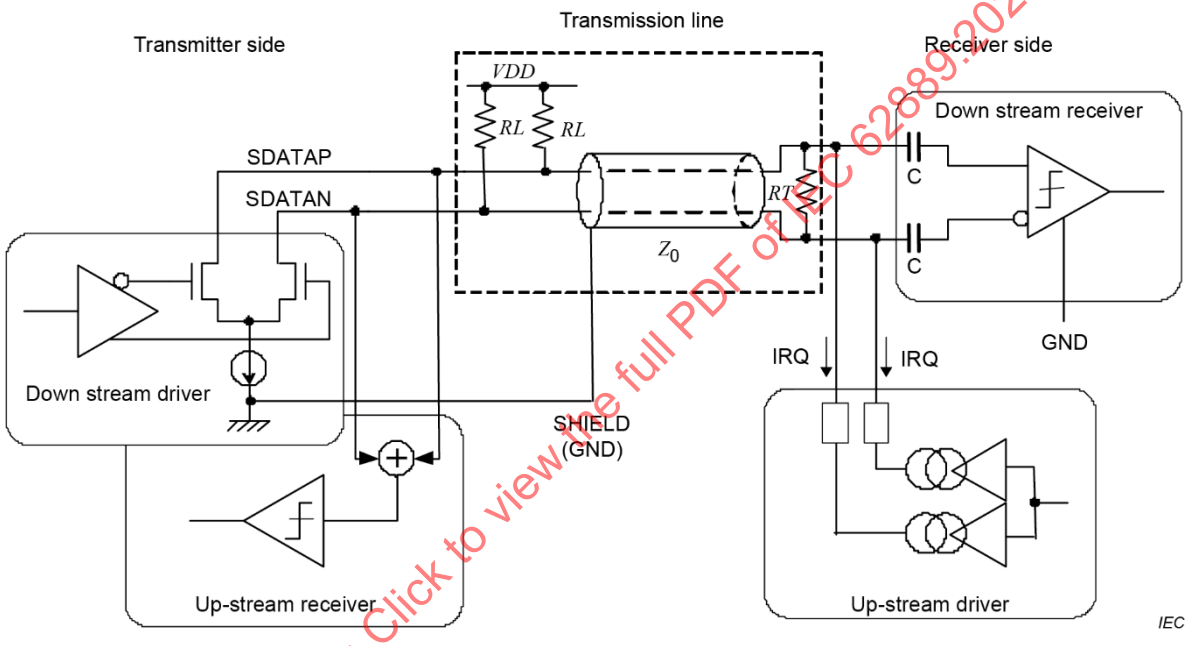


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Figure B.4 – Front-end block diagram

B.3.2 TX front-end

The TX front-end consists of a termination circuit, a downstream driver and an upstream receiver. The termination circuit consists of 2 resistors RL, and the SDATAP/N differential signal is pulled up to voltage reference (VDD) with a (50 ± 15) Ω resistor. The downstream driver consists of a differential current output circuit that is driven by the serial signal from the encoder. The up-stream receiver detects the common-mode signal which RX sends through the shielded twisted-pair line. The input to the downstream driver has two modes. One is the serialized actual encoded video data input mode and the other is the reference clock signal for REFREQ handshake input mode. These two modes activate depending on the common-mode signal level. The common-mode signal level is normally high. When a long low-level pulse is detected, the upstream receiver activates the REFREQ signal, and changes a mode of the encoder into the reference clock mode. In the case of the optional upstream user data transmission, the upstream receiver outputs the common-mode voltage as a UDA signal by using binary digital data sent to the encoder. In this case, the upper limit of the low-pulse time is 100 µs.

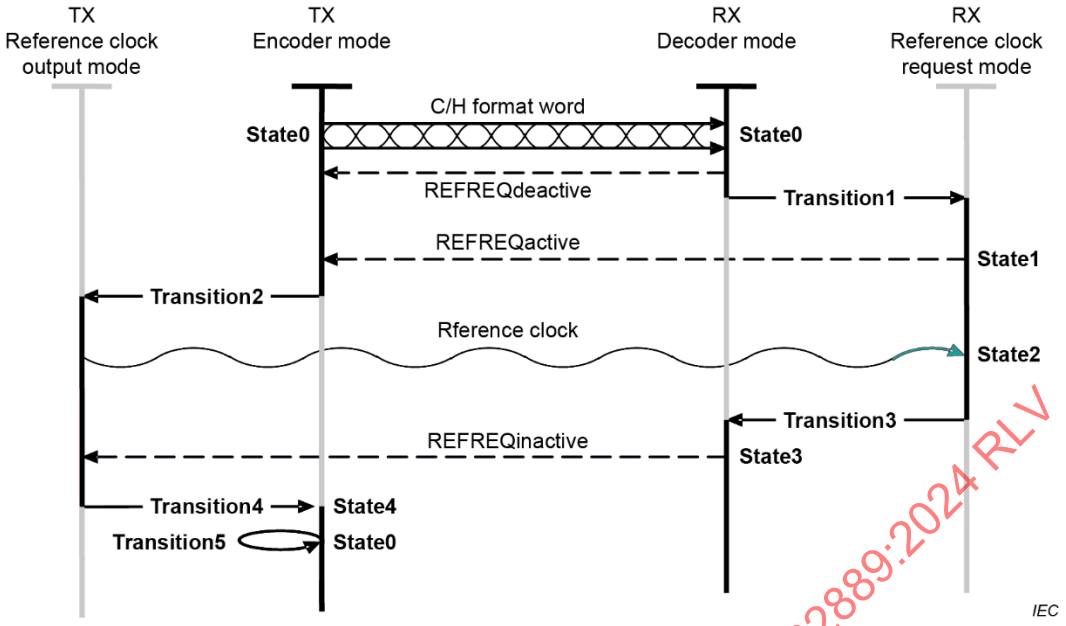
B.3.3 RX front-end

The RX front-end consists of AC capacitors, a termination resistor RT (100 ± 5) Ω, a downstream receiver and an upstream driver. The downstream receiver consists of a differential input detection circuit, which receives the transmission potential differential signal through the shielded twisted-pair line. The upstream driver drives the upstream transmission signal applying a current through the termination resistor RX through the shielded twisted-pair transmission line. A recommended transmission system and transmission line for electrical characteristics is specified in Clause B.2.

B.4 Transition state link

The transition state link of GVIF shall meet the procedure described below.

There are two states in the connection link between GVIF TX and GVIF RX. One is the state transmitting differential signal with a reference clock, the other is the state transmitting the H-format word or the C-format word. In the former state, the TX encoder is in the reference clock output mode and the RX decoder is in the reference clock request mode. In the latter state, the TX encoder changes into the encoder mode and the RX decoder changes into the decoder mode. The state transition switching diagram of the encoder and the decoder is shown in Figure B.5.



State0 (normal)	:	The C/H format word is transmitted down from the TX in the encoder mode to the RX, and the deactivation signal REFREQ is transmitted from the RX in the decoder mode to the TX.
Transition1	:	Transition to the reference clock request mode after finding an irregular HSYNC when the RX decodes.
State1	:	The RX transmits up the activate signal REFREQ.
Transition2	:	The TX transits to the reference clock output mode when the activate signal REFREQ is detected.
State2	:	The TX transmits down the reference clock, and the RX adjusts the internal sampling clock.
Transition3	:	The RX transits to the decoder mode after the internal sampling clock adjustment.
State3	:	The RX transmits up the inactivate signal REFREQ.
Transition4	:	The TX transits to the encoder mode when the inactivate signal REFREQ is detected.
State4	:	P[23:0] transmits continuously the H/C format word equivalent all zero until the TX transmits (VSYNX, HSYNC) (1,1) → (1,0) 60 times.
Transition5	:	Return to normal when the signal has been transmitted 60 times.

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Figure B.5 – Transition state link

B.5 Protocol

B.5.1 General

The encoder encodes the 30 bits of data (P[23:0], HSYNC, VSYNC, DE, CNTL, SDA and TDA) in synchronization with the input of SFTCLK, and outputs 1 bit of the serial signal S to the TX front-end.

To ensure the DC balance data and a reasonable transition, it is required to generate a synchronization pattern for each word in synchronization with the falling edge of HSYNC at the receiver.

B.5.2 Encoder

The encoder encodes the full 30 bits of input data (P[23:0], HSYNC, VSYNC, DE, CNTRL, SDA and TDA) synchronized with SFTCLK, and outputs a 1-bit serial signal S to the TX front-end. The signal is coded after dividing into the following data:

a) Broadband data P[23:0] (24 bits), no transition data.

b) Time mark data HSYNC, VSYNC, DE, CNTL, SDA and TDA (6 bits).

Transition frequency of the signal is limited by the logical specification coding.

The broadband data are normally converted to 1-bit data, but in the case of the time mark data, the transition is converted to 1-bit data. When there is no transition in the time mark data, the broadband data are converted to the C format with 20 % overhead. When there is a time mark transition, the broadband data are converted to the H format with a 6-bit header and 24-bit broadband data.

The broadband data and the time mark data are output as a serial signal S led by the MSB after conversion into a 30-bit length C-format word or H-format word.

The C-format word is used when there is no time mark data transition at the previous pixel clock cycle, and the H-format word is used when there is/are one or more time mark data transition(s) at the previous pixel clock cycle (see Figure B.6).

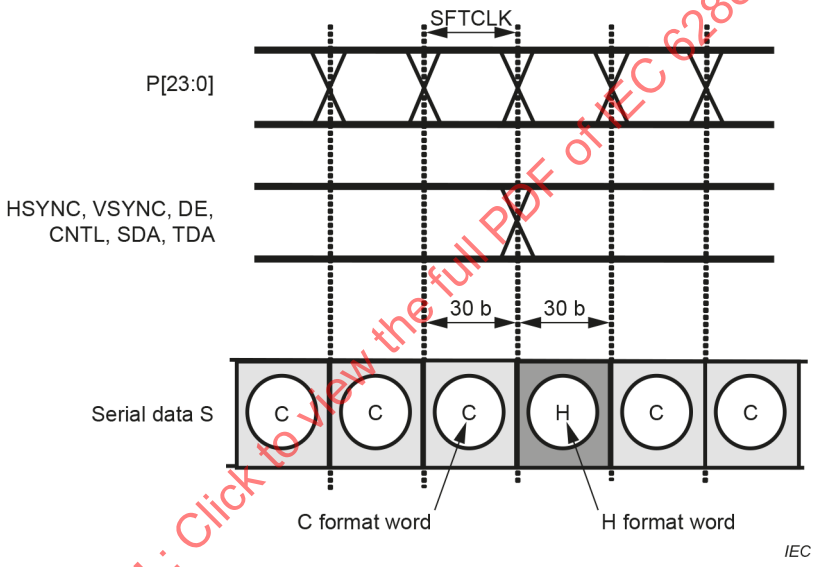

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Figure B.6 – Encoder output diagram

The C-format word consists of the combined six codes of 5 bits which is generated by the 4B/5B conversion (see Table B.5), braking the broadband data P[23:0] by 4 bits (see Figure B.7).

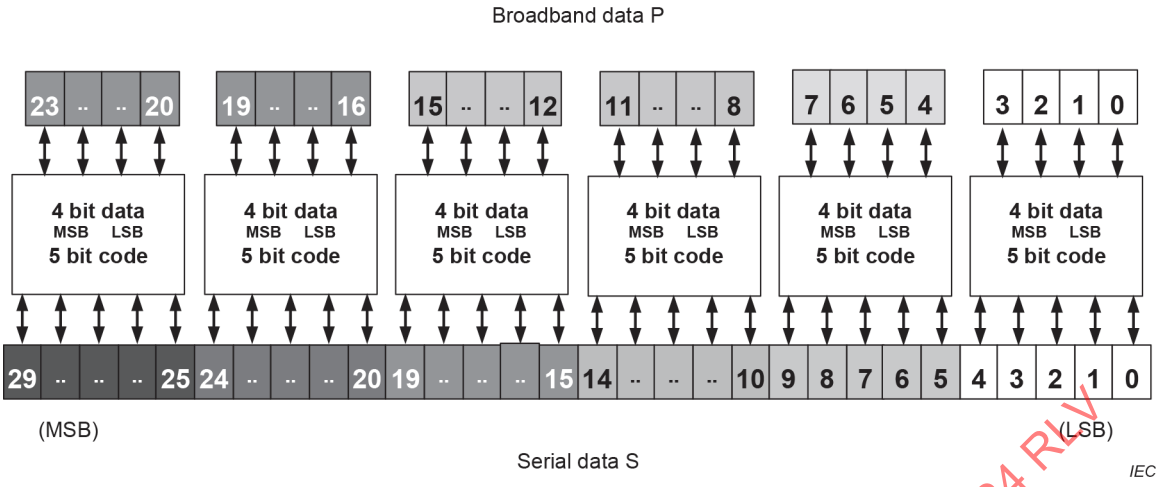

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Figure B.7 – C-format word

Table B.5 – 4B/5B conversion

4-bit data MSB – LSB	5-bit code MSB – LSB	4-bit data MSB – LSB	5-bit code MSB – LSB
"0 0 0 0"	"0 0 1 1 0"	"1 0 0 0"	"1 0 0 1 0"
"0 0 0 1"	"0 0 1 1 1"	"1 0 0 1"	"1 0 0 1 1"
"0 0 1 0"	"0 1 0 0 1"	"1 0 1 0"	"1 0 1 0 0"
"0 0 1 1"	"0 1 0 1 0"	"1 0 1 1"	"1 0 1 0 1"
"0 1 0 0"	"0 1 0 1 1"	"1 1 0 0"	"1 0 1 1 0"
"0 1 0 1"	"0 1 1 0 1"	"1 1 0 1"	"1 1 0 0 1"
"0 1 1 0"	"0 1 1 1 0"	"1 1 1 0"	"1 1 0 1 0"
"0 1 1 1"	"0 1 1 1 1"	"1 1 1 1"	"1 1 1 0 0"
Reproduced from JEITA CP-6101B, Table B-1, with permission from JEITA.			

The H format is generated by a combination of the 24-bit broadband data P[23:0] with a 6-bit header that indicates the transition state of a time mark (see Figure B.8). The positions of even numbers of the broadband data P are inverted in the serial data S. The structure of the header is shown in Table B.6.

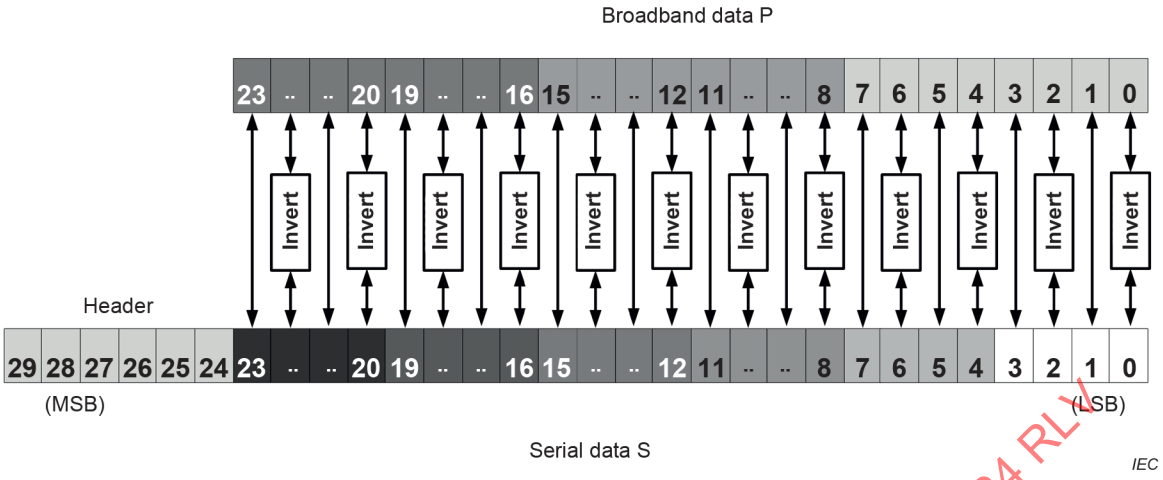

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Figure B.8 – H-format word

Table B.6 – VSYNC, HSYNC, DE, CNTL/AUX, SDA, TDA transition and the corresponding header

	Transition signal	Header bit array	Remark
a	VSYNC, HSYNC	"1 0 0 0 V H"	V and H are the VSYNC inversion value and the HSYNC value after transition.
b	DE, CNTL/AUX	"0 1 1 1 D C"	D and C are the DE and CNTL values after transition.
c	SDA, TDA	"1 1 1 1 S T"	S and T are the SDA and TDA values after transition.
Transition between the signals simultaneously among a, b and c shall not be permitted. Reproduced, with modifications, from JEITA CP-6101B, Table B-2, with permission from JEITA.			

B.5.3 Decoder

The serial data S that comes from the RX front-end is converted as shown in Figure B.7, Figure B.8, Table B.5 and Table B.6.

B.6 Transmission system and transmission line of electrical characteristics

The transmission systems (see Figure B.9) are required to meet the specifications below.

- The differential impedance shall meet the specification stated in Figure B.10. A transmission line has a small and gradual attenuation.
- A transmission line loss on a cable shall be less than −15 dB at 1 GHz in accordance with $\sqrt{f}$ attenuation (see Figure B.11).

The differential signal cable skew time shall be:

- less than 30 % of one bit time (SFTCLK > 33 MHz);
- less than 24 % of one bit time (SFTCLK ≤ 33 MHz).

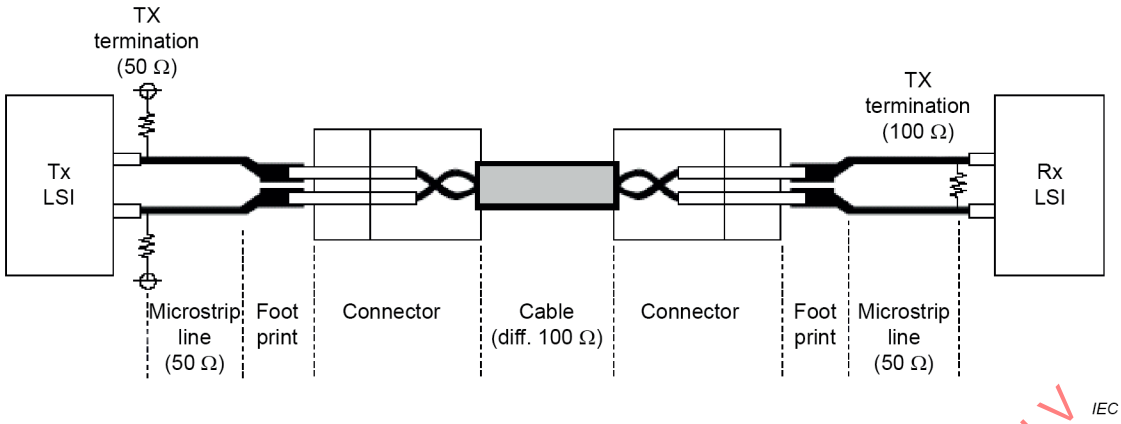

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Figure B.9 – Transmission system

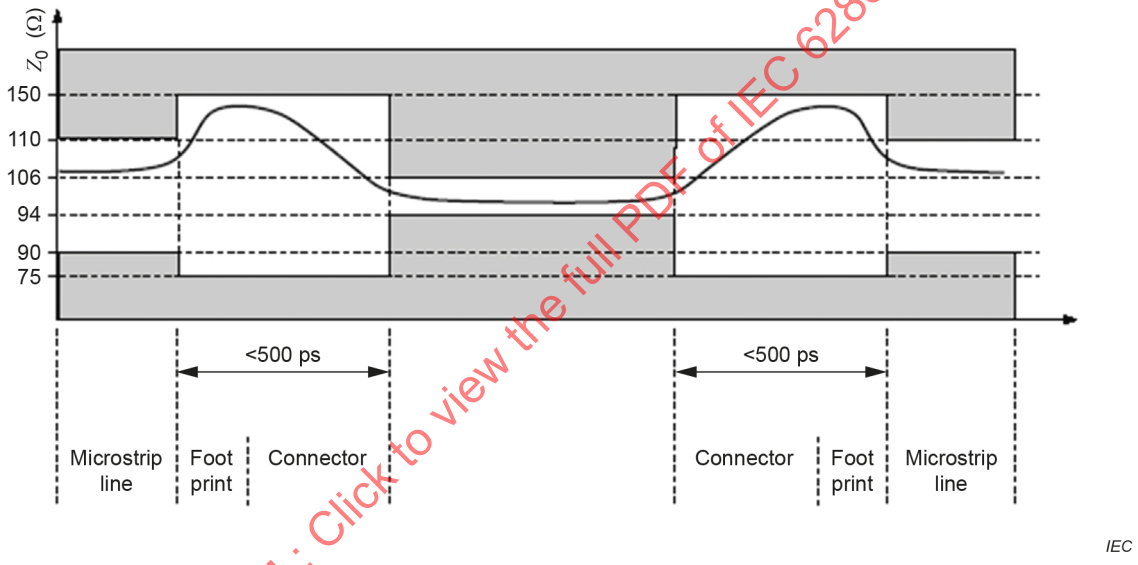

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Figure B.10 – Transmission line tolerance impedance

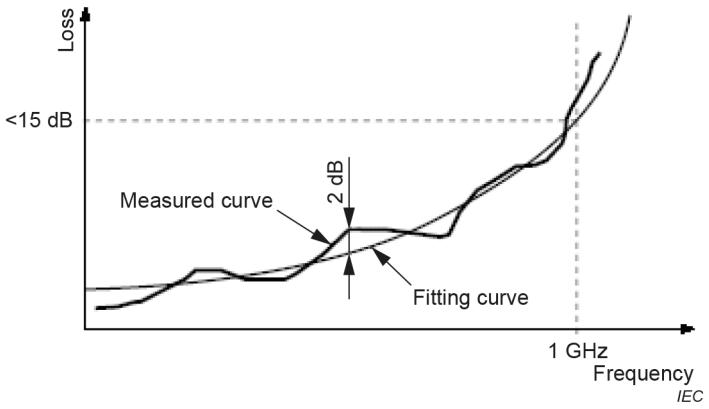

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Figure B.11 – Transmission loss

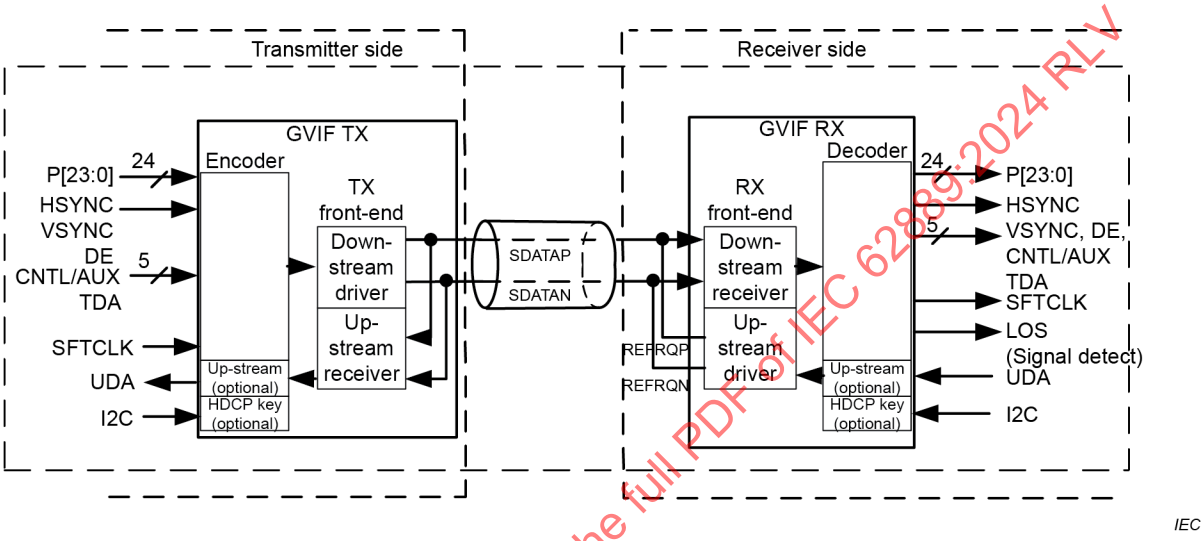
Annex C
(informative)

GVIF Multiple link application

C.1 Single-link application example

C.1.1 Block diagram for single-link transmission

A block diagram of a differential single link is shown in Figure C.1.



Reproduced, with modifications, from JEITA CP-6101B, Figure 3-1, with permission from JEITA.

Figure C.1 – Differential single-link block diagram

The downstream transmission signal is the encoded serial P[23:0], HSYNC, VSYNC, DE, CNTL/AUX, SDA and TDA 30-bit data by the GVIF TX encoder. These data are in all of the SFTCLK domains, and they can be regenerated by the GVIF RX decoder. The encoder and decoder perform in accordance with Clause B.5.

The LOS signal output on the receiver side is asserted when GVIF RX receives no differential signal input or the clock and data recovery circuit in GVIF RX does not generate recovered SFTCLK (loss of lock).

There are optional functions for downstream and upstream user-defined signal transmissions with the terminal names CNTL/AUX and TDA for downstream and UDA for upstream, as shown in Figure C.1. AUX can also optionally use an audio-enable signal.

Additionally, HDCP (high-bandwidth digital contents protection) is also defined as an optional function. The I2C inputs for both GVIF TX and GVIF RX are input terminals to control the HDCP authentication function. The SDA (optional) is generated by an I2C signal order, i.e. a signal to exchange a HDCP key between GVIF TX and GVIF RX.

C.1.2 Data mapping of single-link transmission

A data mapping array should be assigned pixel data of an LCD module, as shown in Figure C.2.

(1,1)	(1,2)	(1,3)	(1,4)	
(2,1)	(2,2)	(2,3)	(2,4)	
(3,1)	(3,2)	(3,3)	(3,4)	
(4,1)	(4,2)	(4,3)	(4,4)	

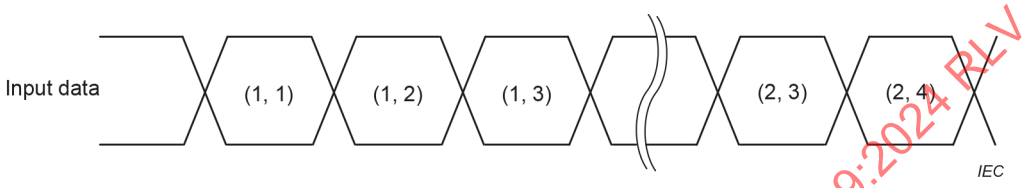


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Figure C.2 – Pixel configuration

C.2 Multiple-link application example

C.2.1 Block diagram for 2-pair parallel transmission

A block diagram of a multiple-link system configuration is shown in Figure C.3. Each channel is called A-channel and B-channel.

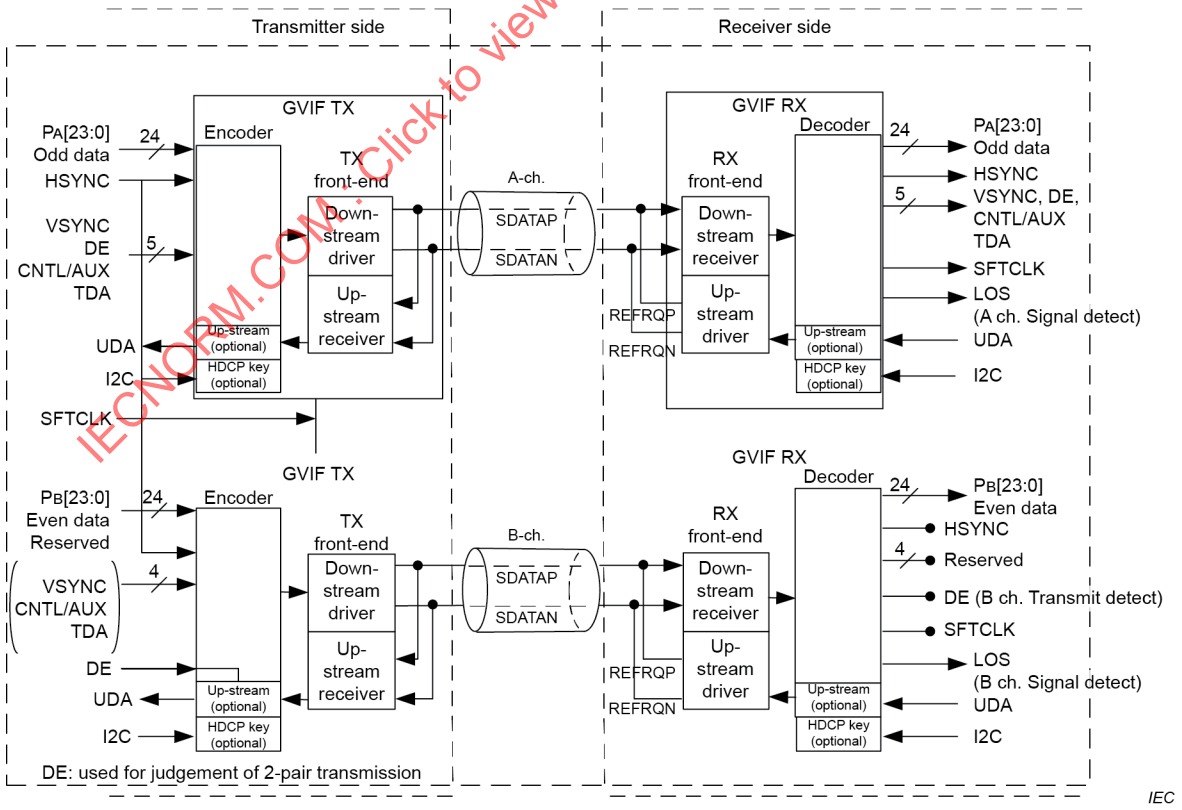

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Figure C.3 – Multiple-link application block diagram

In order to switch between a 1-pair transmission system and 2-pair transmission system, a detection circuit is necessary on the transmitter side. In the case of a 2-pair transmission system, the DE equivalent signal is input to the "DE" pin of the B-ch, and in the case of a 1-pair transmission system, the fixed signal is input to the "DE" pin of the A-ch.

C.2.2 Data mapping of 2-pair transmission

Odd data should be assigned to the A-ch, even data should be assigned to the B-ch.

A data-mapping array for an LCD module is shown in Figure C.4.

(1,1)	(1,2)	(1,3)	(1,4)	
(2,1)	(2,2)	(2,3)	(2,4)	
(3,1)	(3,2)	(3,3)	(3,4)	
(4,1)	(4,2)	(4,3)	(4,4)	
A-ch. data	B-ch. Data	A-ch. data	B-ch. data	

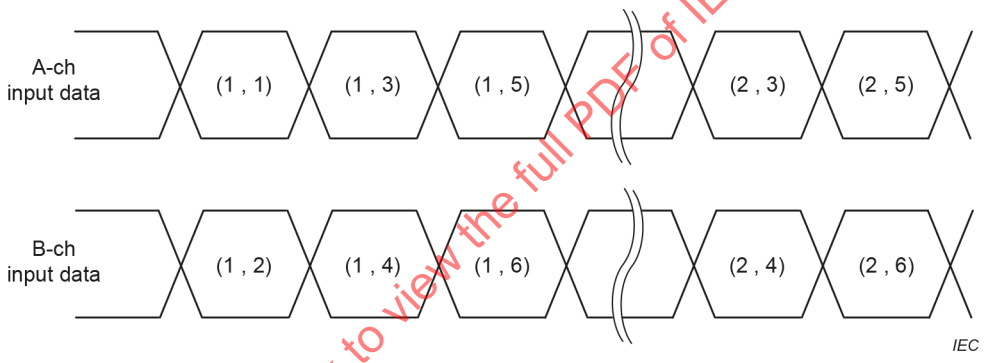

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Figure C.4 – Pixel configuration when using 2-pairs

Bibliography

IEC 62315-1:2003, *DTV profiles for uncompressed digital video interfaces – Part 1: General*

JEITA CP-6101B, Digital monitor interface GVIF, available at *https://www.jeita.or.jp/japanese/standard/book/CP-6101B_J/*

ARIB (Association of Radio Industries and Businesses) STD-B21, *Receiver for Digital Broadcasting (Desirable Specifications)*

ARIB (Association of Radio Industries and Businesses) TR-B14, *Operational Guidelines for Digital Terrestrial Television Broadcasting*

Digital Content Protection LLC, available at http://www.digital-cp.com/

ANSI/TIA/EIA-644-1995, *Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits*, November 1995

I2C-bus specification and user manual Rev. 7.0 –1 October 2021, available at https://www.nxp.com/docs/en/user-guide/UM10204.pdf

SOMMAIRE

COMMISSION ÉLECTROTECHNIQUE INTERNATIONALE

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INTERFACE VIDÉO NUMÉRIQUE – INTERFACE VIDÉO GIGABIT POUR LES SYSTÈMES MULTIMÉDIAS

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Le présent document a été élaboré à partir de la norme JEITA CP-6101B.

Cette deuxième édition annule et remplace la première édition parue en 2015. La présente édition constitue une révision technique.

Cette édition inclut les modifications techniques majeures suivantes par rapport à l'édition précédente:

a) Ajout d'une interface de nouvelle technologie, la GVIF2.

Le texte de cette Norme internationale est issu des documents suivants:

Projet	Rapport de vote
100/3912/CDV	100/4040/RVC

Le rapport de vote indiqué dans le tableau ci-dessus donne toute information sur le vote ayant abouti à son approbation.

La langue employée pour l'élaboration de cette Norme internationale est l'anglais.

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INTRODUCTION

La présente Norme internationale est fondée sur la norme JEITA CP-6101B: *Digital monitor interface GVIF*, initialement définie par la Japan Electronics and Information Technology Industries Association (JEITA).

L'interface vidéo gigabit (GVIF, *Gigabit Video InterFace*) est une interface point à point série qui prend en charge les liaisons vidéo numériques non compressées et qui a été conçue pour répondre entre autres aux besoins des systèmes de navigation et de divertissement automobiles et transporter des informations vidéo numériques en bande de base. La GVIF applique la technologie de signalisation différentielle à basse tension (LVDS, *Low Voltage Differential Signaling*) et utilise un câble fin constitué d'une paire unique de conducteurs torsadés blindés qui présente une haute immunité au bruit et un faible brouillage électromagnétique (EMI, *Electro-Magnetic Interference*), et qui est optimisé pour une petite taille et un faible poids. La GVIF prend en charge les résolutions d'affichage de WQVGA à WUXGA avec des données vidéo couleur de 24 bits par pixel au maximum et peut transmettre un signal vidéo en bande de base sur des longueurs de câble supérieures à 10 m. En option, la GVIF prend en charge la transmission de données audio et la transmission de données utilisateur.

L'interface vidéo gigabit 2 (GVIF2) est une méthode de transmission en bande de base pour les informations vidéo numériques, qui applique la technologie de transmission de données série. Dans la transmission en aval de TX GVIF2 à RX GVIF2, les données de large bande passante pour informations vidéo (GHDS) et le signal de commande du dispositif (GLDS) sont transmis par la méthode du multiplexage temporel. Dans la transmission en amont de RX GVIF2 à TX GVIF2, le signal de commande GLUS est transmis. La transmission en amont et la transmission en aval s'effectuent en duplex intégral. En option, la GVIF2 prend également en charge la transmission de données audio et la transmission de données utilisateur.

Également en option, lorsqu'elles sont associées à une protection des contenus numériques à large bande passante (HDCP, *High-bandwidth Digital Content Protection*), les fonctions et fonctionnalités standards de la GVIF répondent à toutes les exigences relatives à la transmission de contenus vidéo protégés d'une source à un écran d'affichage vidéo.

Le présent document décrit les interfaces de type GVIF. Il traite de la GVIF2 dans le corps principal et l'Annexe A et de la GVIF dans les Annexes B et C.

La GVIF2 présente les fonctionnalités suivantes:

- transmission par un câble à paire différentielle torsadée blindée ou un câble coaxial,
- interface permettant la transmission de contenus vidéo et audio multiples en utilisant le multiplexage temporel,
- possibilité d'utiliser la transmission audio, la communication utilisateur bidirectionnelle et la technologie HDCP (facultatif),
- interface disponible pour la transmission en guirlande (facultatif).

Dans sa norme ARIB STD-B21, l'Association of Radio Industries and Businesses (ARIB) cite la GVIF et la GVIF2 comme étant des interfaces de sortie vidéo numérique autorisées.

INTERFACE VIDÉO NUMÉRIQUE – INTERFACE VIDÉO GIGABIT POUR LES SYSTÈMES MULTIMÉDIAS

1 Domaine d'application

Le présent document décrit deux interfaces numériques série: l'interface vidéo gigabit (GVIF) et l'interface vidéo gigabit 2 (GVIF2), qui permettent l'interconnexion de matériels vidéo numériques. La GVIF et la GVIF2 sont principalement destinées à transporter des données vidéo numériques à grande vitesse pour un usage général et sont bien adaptées aux systèmes de divertissement multimédia pour véhicule.

Le présent document spécifie la couche physique de l'interface, notamment les caractéristiques de la ligne de transmission et les caractéristiques électriques des émetteurs et des récepteurs. Les spécifications mécaniques et physiques des connecteurs ne sont pas incluses.

2 Références normatives

Les documents suivants sont cités dans le texte de sorte qu'ils constituent, pour tout ou partie de leur contenu, des exigences du présent document. Pour les références datées, seule l'édition citée s'applique. Pour les références non datées, la dernière édition du document de référence s'applique (y compris les éventuels amendements).

UIT-R BT.601-5, *Paramètres de codage en studio de la télévision numérique pour des formats standards d'image 4:3 (normalisé) et 16:9 (écran panoramique)*

UIT-R BT.656-5, *Interfaces pour les signaux vidéo numériques en composantes dans les systèmes de télévision à 525 lignes et à 625 lignes fonctionnant au niveau 4:2:2 de la Recommandation UIT-R BT.601*

3 Termes, définitions et abréviations

3.1 Termes et définitions

Pour les besoins du présent document, les termes et définitions suivants s'appliquent.

L'ISO et l'IEC tiennent à jour des bases de données terminologiques destinées à être utilisées en normalisation, consultables aux adresses suivantes:

- IEC Electropedia: disponible à l'adresse https://www.electropedia.org/
- ISO Online browsing platform: disponible à l'adresse https://www.iso.org/obp

3.1.1
DE
signal d'activation d'affichage, selon l'IEC 62315-1

Note 1 à l'article: L'abréviation "DE" est dérivée du terme anglais développé correspondant "display enable".

3.1.2
HSYNC
signal d'affichage synchrone horizontal, selon l'IEC 62315-1

3.1.3
VSYNC
signal d'affichage synchrone vertical, selon l'IEC 62315-1

3.1.4
RGB
affichage d'entrée (TX) ou de sortie (RX) de données de couleur rouge, verte, bleue, selon l'UIT-R BT.601-5 et l'UIT-R BT.656-5

Note 1 à l'article: L'abréviation "RGB" est dérivée du terme anglais développé correspondant "red, green, blue".

3.1.5
CNTL/AUX
signal en aval défini par l'utilisateur ou signal d'activation audio

3.1.6
P[23:0]
données de signal numérique telles que des données vidéo couleur 24 bits, par exemple entrée (TX) ou sortie (RX) de données RGB

3.1.7
GHDS
GVIF2 High bandwidth DownStream
données de contenus en aval de large bande passante du format GVIF2

Note 1 à l'article: L'abréviation "GHDS" est dérivée du terme anglais développé correspondant "GVIF2 High bandwidth DownStream".

3.1.8
GLDS
GVIF2 Low bandwidth DownStream
données des signaux de commande en aval de faible bande passante du format GVIF2

Note 1 à l'article: L'abréviation "GLDS" est dérivée du terme anglais développé correspondant "GVIF2 Low bandwidth DownStream".

3.1.9
GLUS
GVIF2 Low bandwidth UpStream
données des signaux de commande en amont de faible bande passante du format GVIF2

Note 1 à l'article: L'abréviation "GLUS" est dérivée du terme anglais développé correspondant "GVIF2 Low bandwidth UpStream".

3.1.10
RX GVIF
circuit qui reçoit le signal série provenant d'une ligne de transmission à paire blindée, le décode et le convertit en signal vidéo parallèle

3.1.11
TX GVIF
circuit qui reçoit le signal vidéo parallèle et les signaux de commande et les code en données série pour envoyer un signal en pilotant une ligne de transmission à paire blindée

3.1.12
RX GVIF2
circuit qui reçoit le signal série provenant d'un câble à paire torsadée blindée ou d'un câble coaxial, le décode et le convertit en signaux vidéo et audio/de commande

3.1.13
TX GVIF2
circuit qui reçoit les signaux vidéo et audio/de commande, les code en données série et envoie un signal en pilotant un câble à paire torsadée blindée ou un câble coaxial

3.1.14
LOS
perte de détection de signal, affirmé lorsque le signal d'entrée différentiel au niveau du récepteur ne peut pas être reçu

Note 1 à l'article: L'abréviation "LOS" est dérivée du terme anglais développé correspondant "loss of signal".

3.1.15
Front RX
bloc frontal côté récepteur

3.1.16
SDA
signal en aval des données série

Note 1 à l'article: L'abréviation "SDA" est dérivée du terme anglais développé correspondant "serial data".

3.1.17
SDATA
signal des données série de la GVIF2 sur la transmission du câble coaxial

3.1.18
SDATAP
signal latéral de phase positive en aval des données série différentielles

3.1.19
SDATAN
signal latéral de phase négative en aval des données série différentielles

3.1.20
REF
signal de référence

3.1.21
REFRQP
signal positif source de courant pour la demande d'horloge de référence du côté RX

3.1.22
REFRQN
signal négatif source de courant pour la demande d'horloge de référence du côté RX

3.1.23
SFTCLK
horloge de pixel pour la capture des données vidéo parallèles par pixel

3.1.24
TDA
signal en aval défini par l'utilisateur pour la transmission de données

Note 1 à l'article: L'abréviation "TDA" est dérivée du terme anglais développé correspondant "transmit data".

3.1.25
Front TX
bloc frontal côté émetteur

3.1.26
UDA
signal en amont de données auxiliaires défini par l'utilisateur

Note 1 à l'article: L'abréviation "UDA" est dérivée du terme anglais développé correspondant "user data".

3.1.27
IRQ
courant en mode commun de la demande de référence en amont pour REFRQP/N

3.1.28
VOS
amplitude de tension en mode commun de la demande de référence

3.1.29
VOD
amplitude de tension différentielle pour SDATAP/N

3.1.30
VDD
alimentation du côté de l'émetteur

3.1.31
V_SDATAP
tension asymétrique de SDATAP

3.1.32
V_SDATAN
tension asymétrique de SDATAN

3.1.33
TP1
point d'essai d'une spécification du masque de l'œil en aval

3.1.34
TP2
point d'essai d'une spécification du masque de l'œil en amont

3.1.35
tension différentielle normalisée
tension du point de sortie de l'émetteur

3.1.36
UI
intervalle d'unité de temps normalisé du point de sortie de l'émetteur

Note 1 à l'article: L'abréviation "UI" est dérivée du terme anglais développé correspondant "unit interval".

3.1.37
WSYNC
signal synchronisé en mot

3.2 Abréviations

AC alternating current (courant alternatif)

DC direct current (courant continu)

EMI electro-magnetic interference (brouillage électromagnétique)

GVIF Gigabit Video InterFace (interface vidéo gigabit)

HDCP high-bandwidth digital content protection (protection des contenus numériques à large bande passante)

LSB least significant bit (bit de poids faible)

LVDS low voltage differential signaling (signalisation différentielle à basse tension)

MSB most significant bit (bit de poids fort)

PRBS pseudo random binary sequence (séquence binaire pseudo-aléatoire)

4 Architecture

La GVIF2 a une capacité d'interface multimédia supérieure et correspond ainsi à la nouvelle génération de GVIF décrite à l'Annexe B et à l'Annexe C.

La ligne de transmission de la GVIF2 est un câble à paire torsadée blindée d'impédance caractéristique différentielle Z0_diff ou un câble coaxial d'impédance caractéristique Z0_coax, qui est connecté à RX GVIF2 et à TX GVIF2, avec condensateur de couplage en courant alternatif et résistance de terminaison à haute fréquence (voir Figure 1). Le trajet du signal de la ligne de transmission de la GVIF2 est isolé de TX GVIF2 et de RX GVIF2 en courant continu. Le blindage de la ligne de transmission de la GVIF2 est connecté à la terre (GND) du circuit TX et du circuit RX.

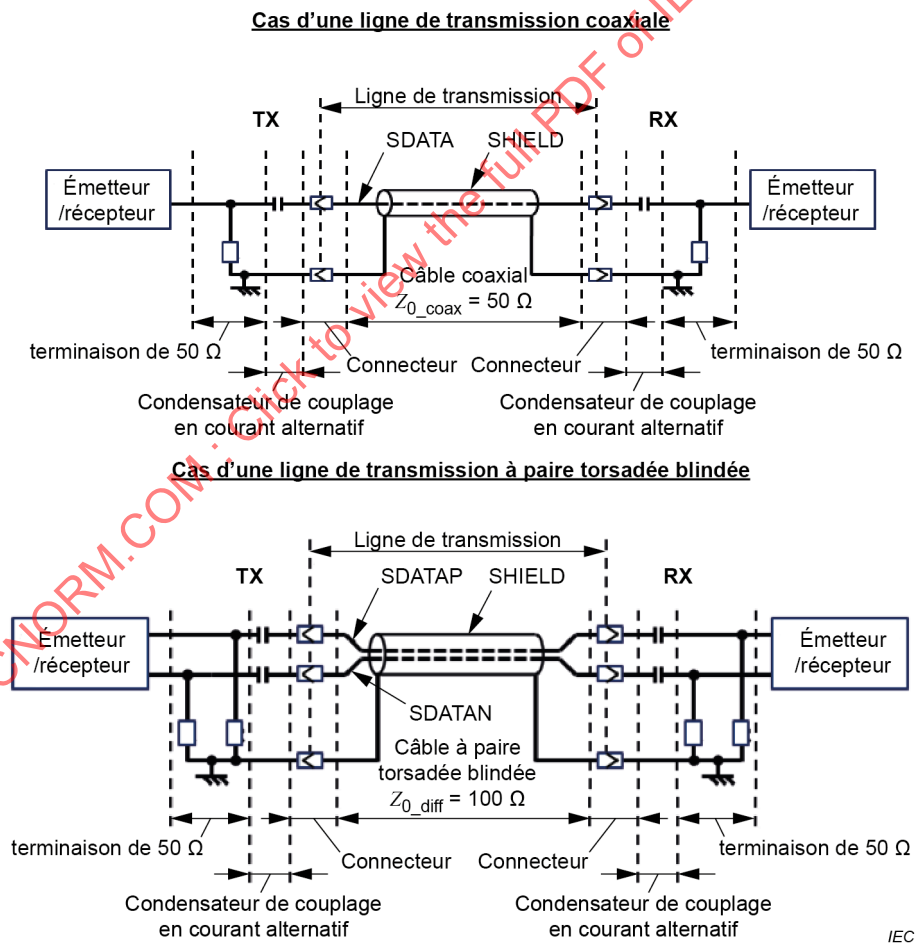

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Figure 1 – Architecture de la GVIF2

5 Caractéristiques électriques

5.1 Généralités

Les spécifications en courant alternatif décrites ci-dessous doivent être satisfaites. Il n'existe pas de spécifications en courant continu pour la GVIF2, car l'architecture de transmission de la GVIF2 est un couplage complet en courant alternatif.

5.2 Spécifications électriques en courant alternatif

Les spécifications électriques en courant alternatif du côté émetteur et du côté récepteur figurent dans le Tableau 1. La définition des niveaux de tension est indiquée à la Figure 2. La Figure 3 et la Figure 4 montrent une spécification du masque de l'œil en aval au TP1 et une spécification du masque de l'œil en amont au TP2 de la GVIF2.

Tableau 1 – Spécifications électriques en courant alternatif de la GVIF2

	Débit binaire en aval			**Débit binaire en amont**
	Fdownstream_1 Gbit/s	**Fdownstream_2** Gbit/s	**Fdownstream_3** Gbit/s	**Fupstream** Mbit/s
Minimum	2,16	3,24	4,32	9,0
Maximum	2,4	3,6	4,8	10,0
Fupstream = Fdownstream_1/240 ou Fupstream = Fdownstream_2/360 ou Fupstream = Fdownstream_3/480				
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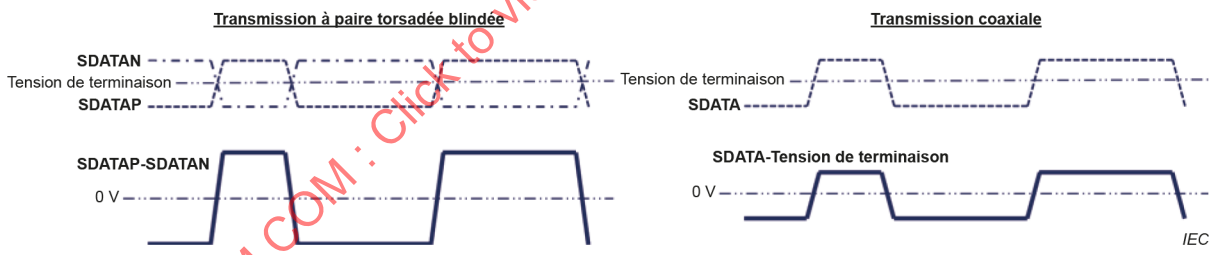

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Figure 2 – Définition des niveaux de la GVIF2

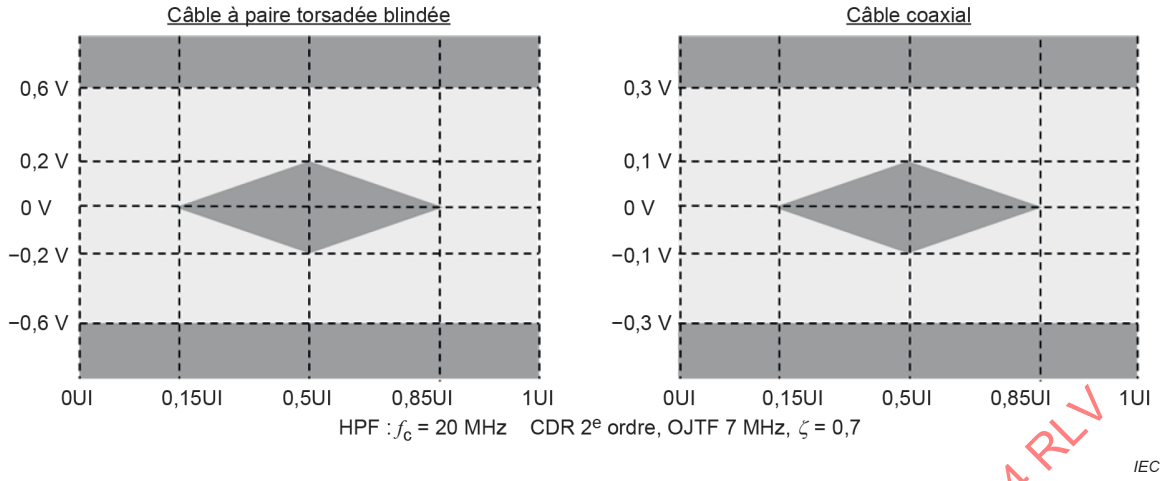

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Figure 3 – Masque de l'œil en aval de la GVIF2 (au TP1)

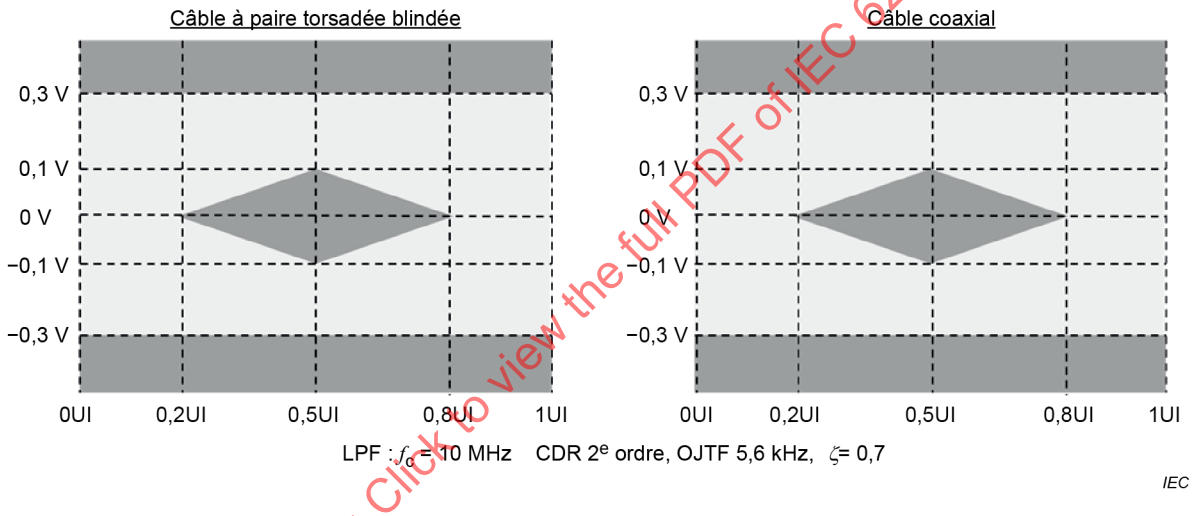

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Figure 4 – Masque de l'œil en amont de la GVIF2 (au TP2)

6 Front

6.1.1 Généralités

Le schéma fonctionnel frontal de la GVIF2 est présenté à la Figure 5.

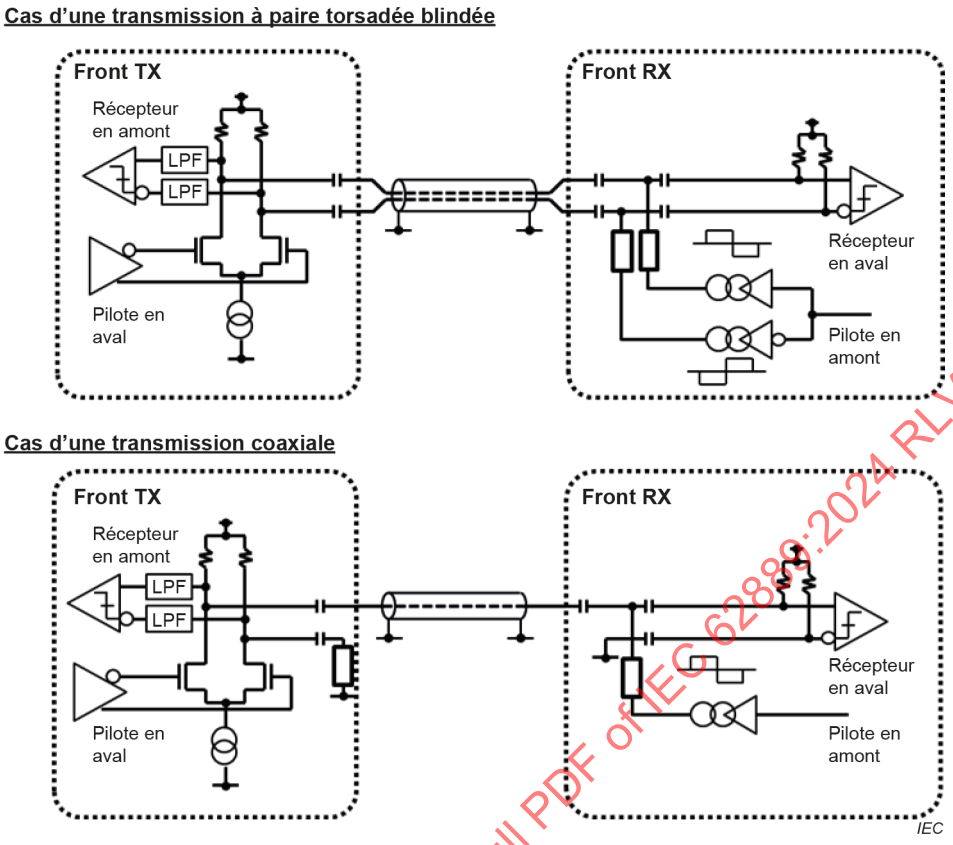

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Figure 5 – Schéma fonctionnel frontal de la GVIF2

6.1.2 Front TX

Le front TX de la GVIF2 est constitué de condensateurs de couplage en courant alternatif, de résistances de terminaison, d'un pilote en aval, d'un récepteur en amont et de connecteurs. Les résistances de terminaison, en tant que charge du courant différentiel du pilote en aval, génèrent la tension de signal en aval et deviennent la terminaison à haute fréquence de la ligne de transmission. Le récepteur en amont reproduit les données extraites par le filtre passe-bas (LPF, *low pass filter*) du signal en amont transmis par RX.

6.1.3 Front RX

Le front RX de la GVIF2 est constitué de condensateurs de couplage en courant alternatif, de résistances de terminaison, d'un récepteur en aval et d'un pilote en amont. Le récepteur en aval reproduit les données du signal en aval qui sont transmises par TX et extraites par le filtre passe-haut (HPF, *high pass filter*), constitué des condensateurs de couplage en courant alternatif et des résistances de terminaison. Le pilote en amont conduit le signal en amont jusqu'à la ligne de transmission via le LPF. Le signal en amont est en synchronisation de fréquence avec le signal en aval et le débit de transmission, proportionnel au débit en aval, est de 10 Mbit/s au maximum.

6.1.4 Schéma fonctionnel de configuration

Le signal en aval est codé en GHDS et GLDS dans le code en aval. Le débit de transmission doit être sélectionné parmi les débits de 2,4 Gbit/s, 3,6 Gbit/s ou 4,8 Gbit/s en fonction de la bande passante requise pour les GHDS.

Les GHDS doivent être réglées par un multiplexage temporel dans les unités DATA SLOT.

Les GHDS peuvent utiliser la transmission de contenus vidéo (et audio) multiples (facultatif, voir Annexe A).

Le signal en amont doit être codé en GLUS dans le code en amont.

L'amont et l'aval doivent être transmis simultanément (duplex intégral) par division de fréquence.

Le mappage des données du schéma fonctionnel de configuration de la GVIF2 est représenté à la Figure 6.

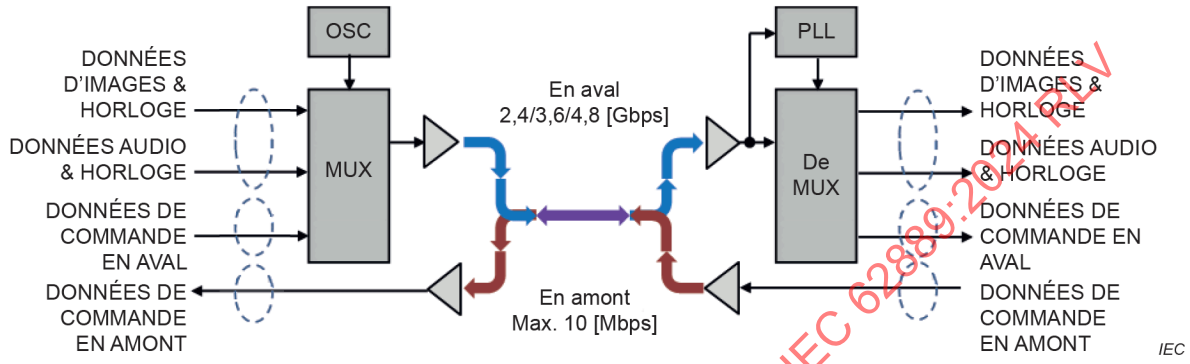

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Figure 6 – Mappage des données du schéma fonctionnel de configuration de la GVIF2

6.1.5 Mappage des données

6.1.5.1 Mappage des données RGB888 pour GHDS

Les données RGB888 et les signaux de synchronisation VSYNC/HSYNC/DE doivent être mappés en GHDS, comme indiqué à la Figure 7.

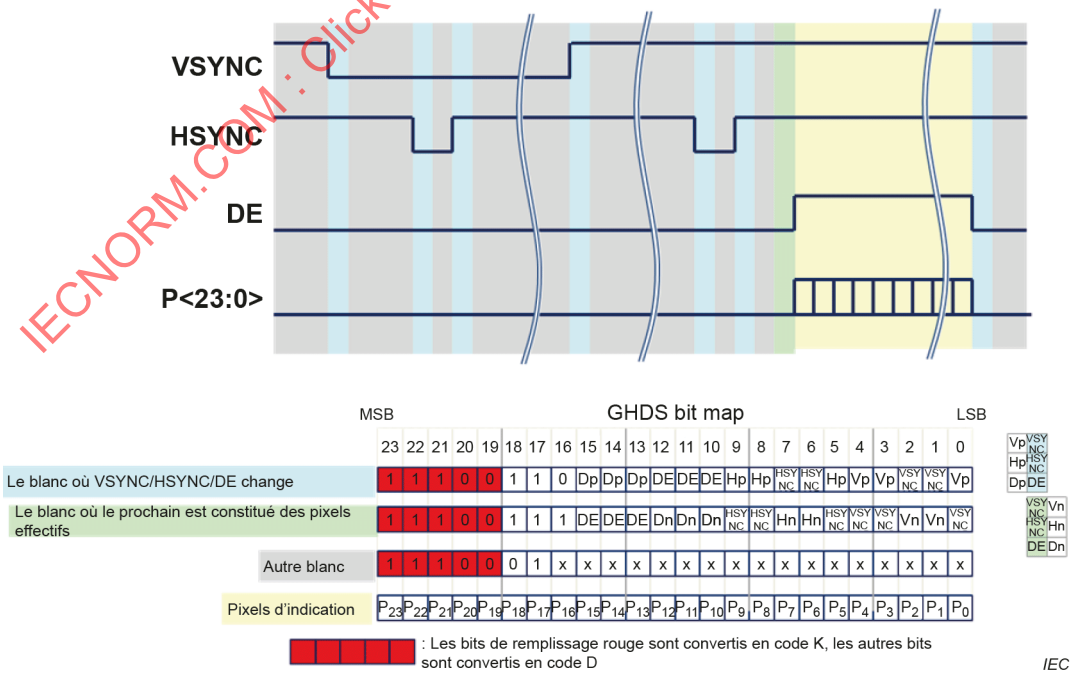

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Figure 7 – Mappage des données RGB888 de la GVIF2

6.1.5.2 Mappage du contenu pour d'autres formats (facultatif)

MAINDATA, MAINCTRL, SUBDATA peuvent être mappés en GHDS suivant l'accord de coordination entre TX GVIF2 et RX GVIF2, comme indiqué à la Figure 8. Le mappage des données vidéo pixel MAINDATA, des signaux de synchronisation vidéo en MAINCTRL et des signaux audio (facultatif) en SUBDATA est recommandé.

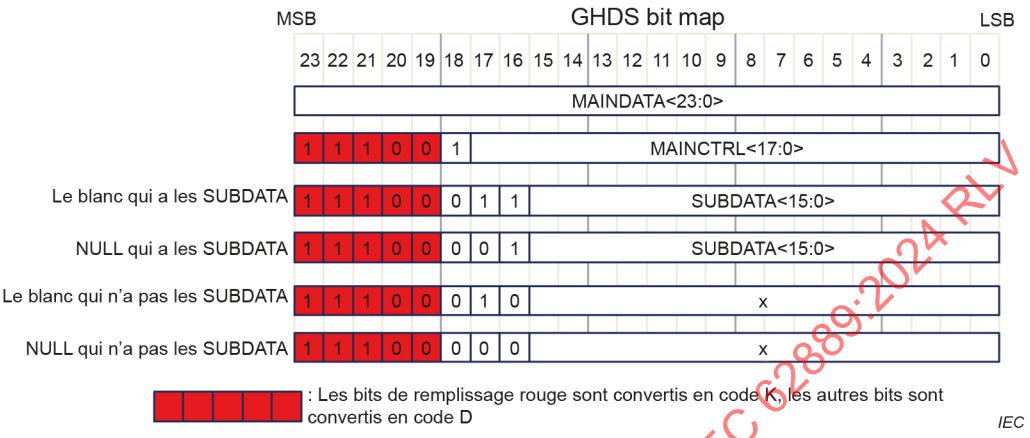

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Figure 8 – Mappage des données de contenus généraux de la GVIF2 (facultatif)

Les signaux de communication bidirectionnelle entre TX GVIF2 et RX GVIF2 tels que UART peuvent être mappés en GLDS et GLUS (facultatif).

Le mappage des données de certification HDMI (HDCP) en SUBDATA, GLDS, GLUS et une partie de GHDS est recommandé (facultatif).

7 Liaison d'état de transition

Le schéma fonctionnel des états de transition de TX GVIF2 et de RX GVIF2 est présenté à la Figure 9.

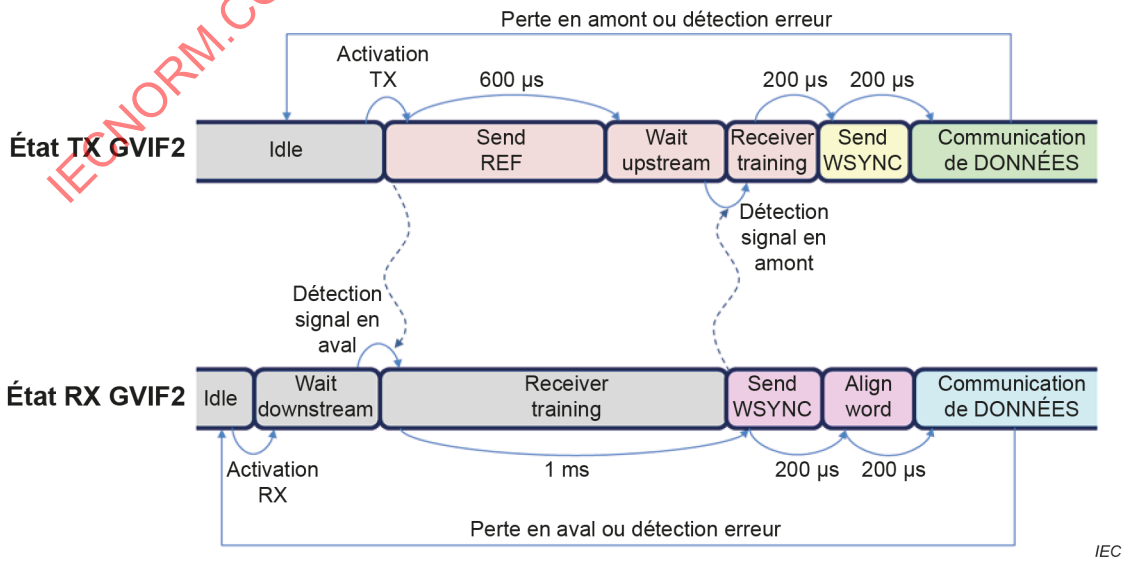

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Figure 9 – Schéma fonctionnel des états de transition de la GVIF2

Dans TX GVIF2 connecté à RX GVIF2, il existe plusieurs états, dont un état sans signal en aval (Idle), des états transmettant un signal REF (Send REF, Wait Upstream, Receiver Training), un état transmettant un signal SYNC (Send WSYNC) et un état de transmission en aval normal. Alors qu'il doit passer de "Idle" à "Send REF" lorsque le circuit TX est activé et de "Wait Upstream" à "Receiver Training" lorsque le signal en amont est détecté, les autres transitions doivent impérativement s'effectuer dans l'intervalle de temps spécifié. Si le signal en amont n'est pas détecté dans l'état de transmission en aval normal ou si une erreur est détectée dans le signal en amont, il doit passer à "Idle".

Dans RX GVIF2 connecté à TX GVIF2, il existe plusieurs états, dont un état sans signal en amont (Idle, Wait Downstream, Receiver Training), des états transmettant un signal SYNC (Send WSYNC, Align Word) et un état de transmission en amont normal. Alors qu'il doit passer de "Idle" à "Wait Downstream" lorsque le circuit RX est activé et de "Wait Downstream" à "Receiver Training" lorsque le signal en aval est détecté, les autres transitions doivent impérativement s'effectuer dans l'intervalle de temps spécifié. Si le signal en aval n'est pas détecté dans l'état de transmission en amont normal ou si une erreur est détectée dans le signal en aval, il doit passer à "Idle".

La sortie des signaux REF et WSYNC en aval provenant de TX GVIF2 doit être les GHDS et GLDS codés (voir Figure 10).

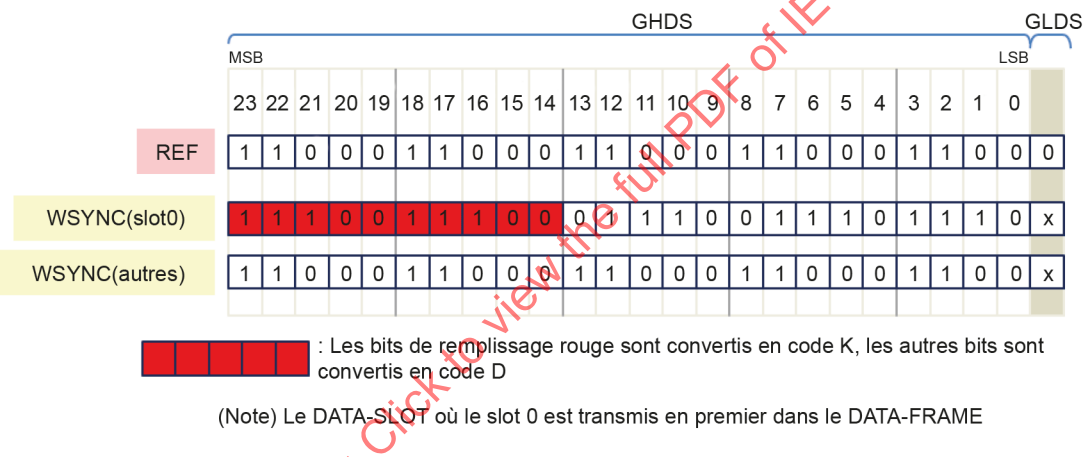

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Figure 10 – Signaux REF et WSYNC de la GVIF2 en aval

La sortie du signal WSYNC en amont provenant de RX GVIF2 doit être les GLUS codés (voir Figure 11).

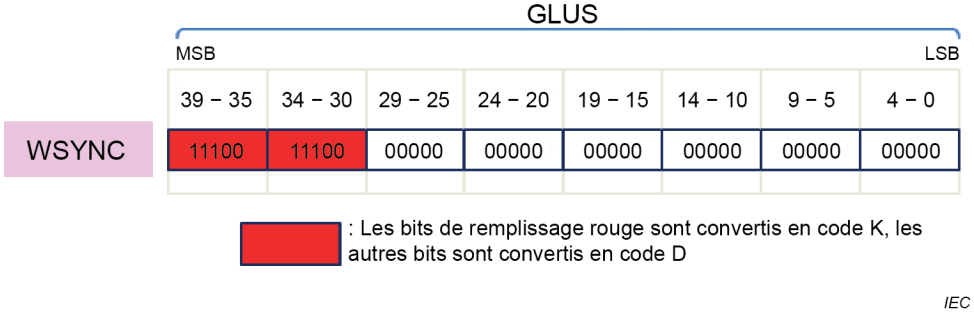

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Figure 11 – Signal WSYNC en amont