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Edition 1.0 2022-12

INTERNATIONAL STANDARD

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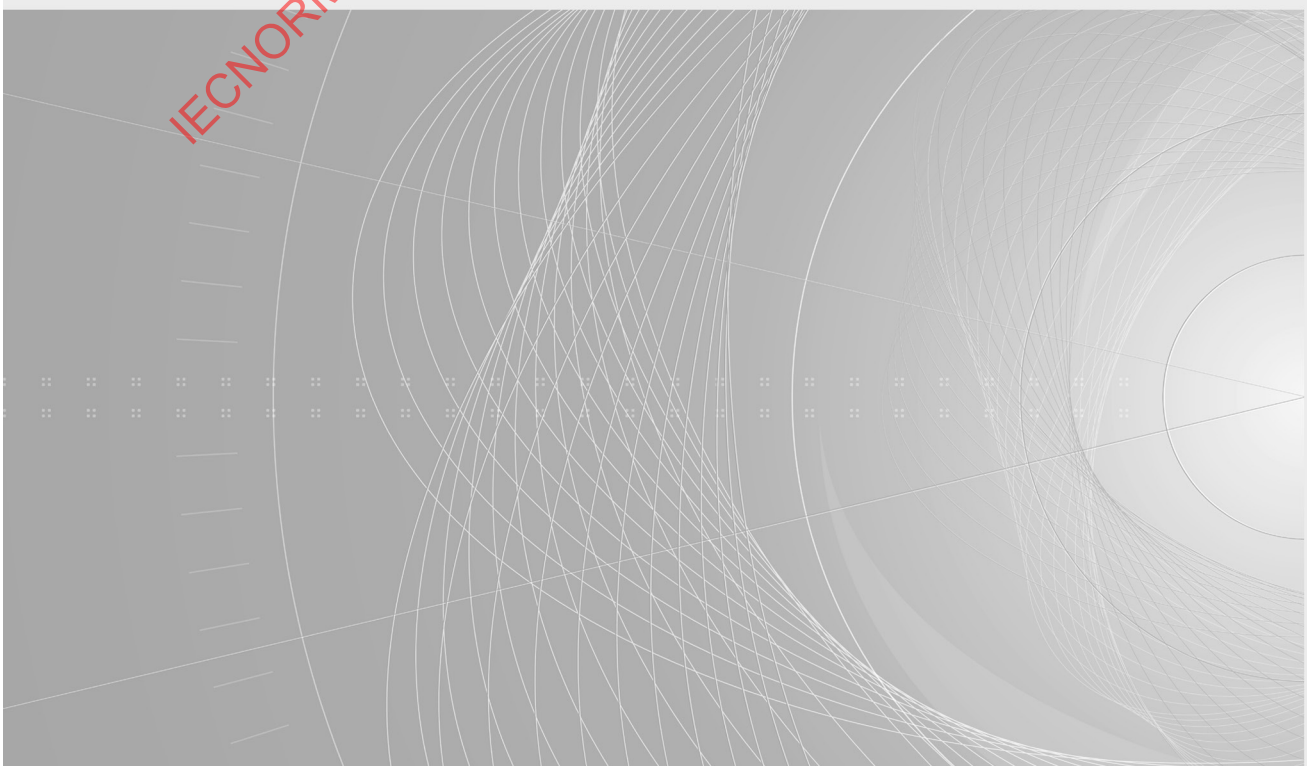
Semiconductor devices – Flexible and stretchable semiconductor devices – Part 9: Performance testing methods of one transistor and one resistor (1T1R) resistive memory cells



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IEC Secretariat
3, rue de Varembé
CH-1211 Geneva 20
Switzerland

Tel.: +41 22 919 02 11
info@iec.ch
www.iec.ch

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Part 9: Performance testing methods of one transistor and one resistor (1T1R) resistive memory cells

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Draft	Report on voting
47/2781/FDIS	47/2791/RVD

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/standardsdev/publications.

A list of all parts in the IEC 62951 series, published under the general title *Semiconductor devices – Flexible and stretchable semiconductor devices*, can be found on the IEC website.

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SEMICONDUCTOR DEVICES – FLEXIBLE AND STRETCHABLE SEMICONDUCTOR DEVICES –

Part 9: Performance testing methods of one transistor and one resistor (1T1R) resistive memory cells

1 Scope

This part of IEC 62951 specifies the test methods for evaluating the performance of unipolar-type one transistor one resistor (1T1R) resistive memory cells. The performance test methods in this document include read, forming, SET, RESET, endurance and retention. This document is applicable to flexible devices as well as rigid resistive memory devices without any limitations prone to device technology and size.

2 Normative references

There are no normative references in this document.

3 Terms and definitions

For the purpose of this document, the following terms and definitions apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at http://www.electropedia.org/
- ISO Online browsing platform: available at http://www.iso.org/obp

3.1
programming transistor
semiconductor device used to amplify, limit or switch electronic signals and electrical power

3.2
source voltage
V_S
bias applied to the source terminal of the programming transistor

3.3
gate voltage
V_G
bias applied to the gate terminal of the programming transistor

3.4
drain voltage
V_D
bias applied to the drain terminal of the programming transistor

3.5
resistive memory
two terminal device, based on reversible formation and rupture of filament within active layer, defining low and high resistance states, respectively

3.6
forming voltage
V_{Form}
high voltage applied across the active layer to induce defects within the active layer to for a filament or conduction path initially

3.7
resistance of low resistance state
R_{LRS}
resistance of memory device in SET state

3.8
resistance of high resistance state
R_{HRS}
resistance of memory device in RESET state

3.9
trip point resistance
R_{TRP}
intermediate reference resistance between R_{HRS} and R_{LRS}

$$R_{HRS} > R_{TRP} > R_{LRS}$$

3.10
step voltage
V_{Step}
ramp of voltage intervals applied to resistive memory

3.11
read voltage
V_{Read}
specific voltage for measuring the resistance of resistive memory, R_R

3.12
read current
I_{Read}
specific current value at V_{Read} for measuring the resistance of resistive memory, R_R

3.13
resistance of resistive memory
R_R
resistance value at V_{Read}, defined by the following formula

$$R_R = \frac{V_{Read}}{I_{Read}}$$

3.14
SET voltage
V_{SET}
voltage required to switch resistive memory to R_{LRS} after forming process

3.15
RESET voltage
V_{RESET}
voltage required to switch resistive memory to R_{HRS}

3.16
SET time
t_{SET}
time required to switch resistive memory to R_{LRS}

3.17
RESET time
t_{RESET}
time required to switch resistive memory to R_{HRS}

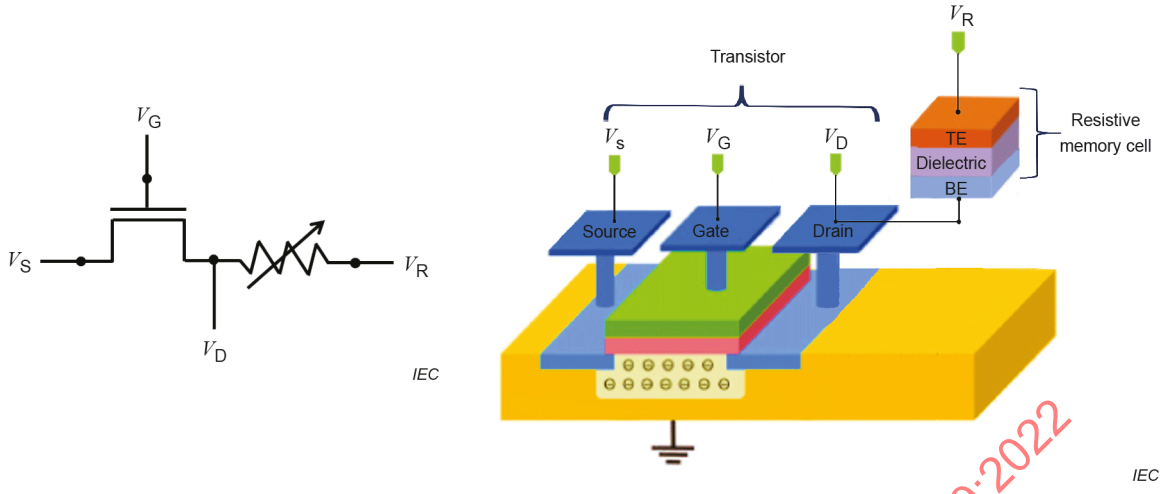
3.18
programming transistor on voltage
V_{ON}
voltage required to turn on programming transistor

3.19
delay time
t_{Delay}
required time between V_R and V_G for stable operation

3.20
pulse width
t_R
elapsed time between the rising and falling edges of a single pulse

4 Device under testing (DUT)

Figure 1 a) shows the equivalent circuit of 1T1R resistive memory cell. The top electrode of the resistive memory, the source, gate and drain of the transistor are defined as terminal V_R, V_S, V_G and V_D, respectively. Figure 1 b) shows the schematic diagram of 1T1R resistive memory cell. The resistive memory is integrated on the drain-side of the transistor. Different voltage biases are applied to each terminal during forming, SET and RESET operations.



a) Equivalent circuit **b) Schematic diagram**

Figure 1 – 1T1R resistive memory cell

Resistive memory is composed of an insulating oxide material sandwiched between two metal electrodes. The bottom electrode (BE) of the cell is connected to the drain of transistor. The V_R is applied on the top electrode of the 1T1R resistive memory cell with V_S grounded. The transistor limits the current during the forming and SET operations by the gate voltage, V_G.

5 Test method

5.1 General

Test procedures for 1T1R resistive memory cells are performed as shown in Figure 2. First, 1T1R resistive memory cell (DUT) is mounted on a test fixture, and its electrical characteristics are measured by varying voltage, current and temperature. For measuring and characterizing these devices accurately, ultra-high accuracy sensors shall be employed.

5.2 Test equipment and tools

5.2.1 General

A variety of experimental approaches have been employed to test 1T1R resistive memory cells. Semiconductor parameter analyzer is a test instrument that integrates multiple measurement and analysis capabilities to perform the current-voltage (I-V) and capacitance measurements (C-V (capacitance-voltage), C-f (capacitance-frequency), and C-t (capacitance-time)) of 1T1R resistive memory cells. The semiconductor parametric test is a fundamental measurement to determine the characteristics of a semiconductor device and its manufacturing process.

The key measurement component of the parameter analyzer is a source measure unit (SMU). The SMU is a measurement module that combines the capabilities of a voltage/current source and a voltage/current meter into a single module. Because the source and measurement circuitry are closely integrated, one can achieve far better accuracy and higher resolution with less measurement error than using various independent instruments to make the same measurement. To perform ultra-fast (transient) I-V measurements, the pulse generator unit (PGU) provides ultra-fast voltage waveform generation and signal observation on different channels of integrated sourcing and measurement. Hot chuck is also an important tool to be used together with a prober for evaluating temperature characteristics of 1T1R resistive memory cells.

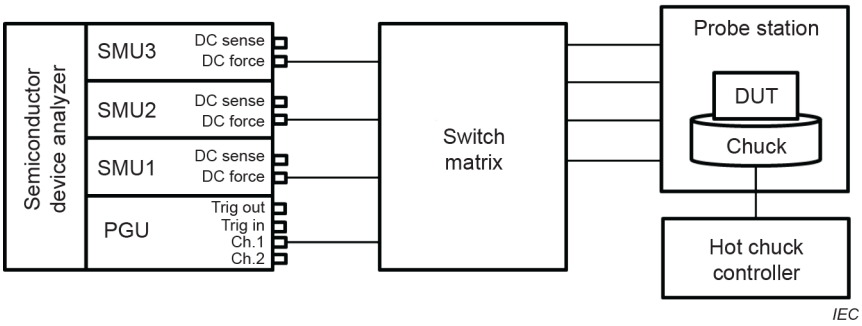
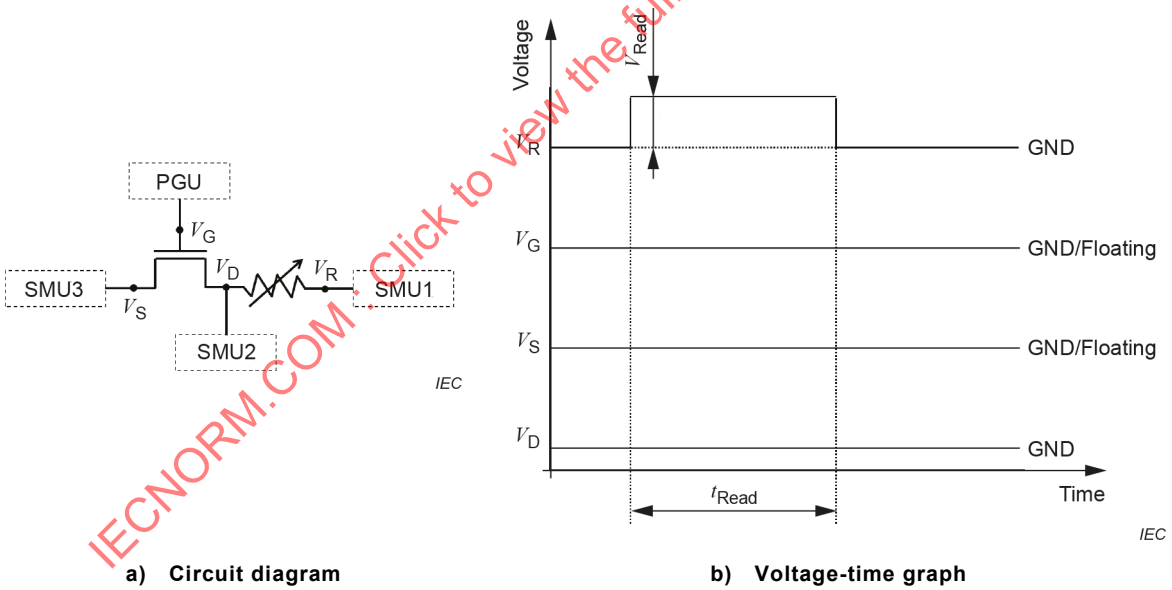


Figure 2 – Block diagram of the measurement setup of 1T1R resistive memory cells

5.2.2 Read

Figure 3 a) corresponds to the circuit diagram and Figure 3 b) corresponds to the voltage-time graph to exhibit the read operation of 1T1R resistive memory cell. The current value, I_{Read}, is measured to calculate the resistance of resistive memory, R_R, when V_{Read} with pulse width t_{Read} is applied across the resistive memory.

Figure 4 shows the exemplary cumulative probability distribution of HRS and LRS of 1T1R resistive memory cells with intermediate resistance trip point resistance, R_{TRP}. To be considered as an application for the field case, R_{HRS}/R_{LRS} in Figure 4 should be equal to or greater than 2.



a) Circuit diagram **b) Voltage-time graph**

Figure 3 – Read operation of 1T1R resistive memory cell

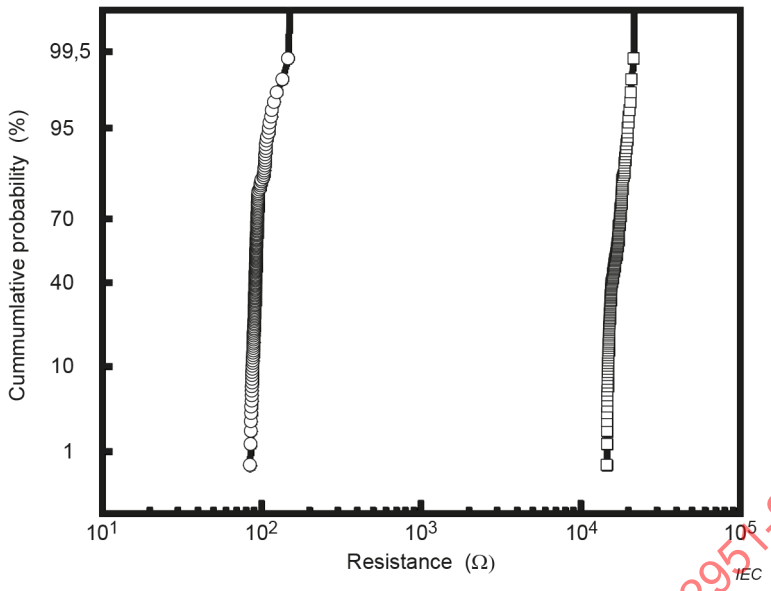
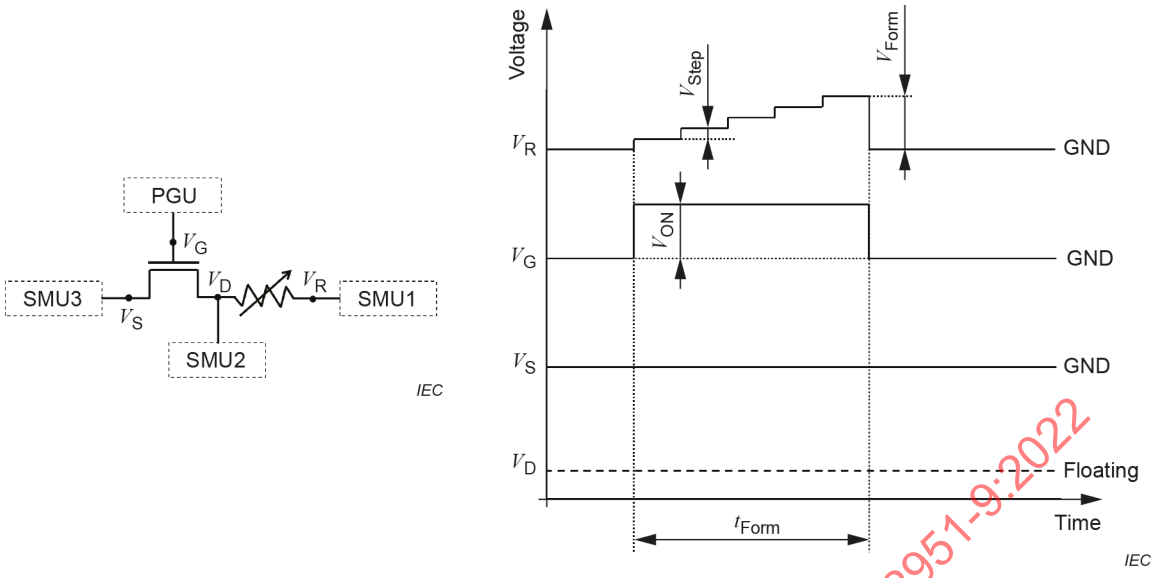


Figure 4 – Cumulative probability distribution of HRS and LRS of 1T1R resistive memory cells

5.2.3 Forming

Figure 5 a) shows the circuit diagram and Figure 5 b) shows the voltage-time graph to exhibit the forming operation of 1T1R resistive memory cell. As shown in Figure 5, V_{Step} is applied on the top electrode of 1T1R resistive memory cells. As soon as the filament is formed at V_{Form}, electrically connecting the two electrodes, the current limit is fixed by the programming transistor which stops the permanent breakdown of the dielectric layer between the two electrodes. The programming current level is modulated by the gate voltage, V_{G}. V_{S} of the programming transistor is grounded during the forming operation.

The simulation test flow chart in Figure 6 shows that before applying the forming voltage, the pristine resistance R_{R} of the device is read; if it is in the R_{HRS}, the forming operation is initiated to achieve the SET state.



a) Circuit diagram **b) Voltage-time graph**

Figure 5 – Forming operation of 1T1R resistive memory cell

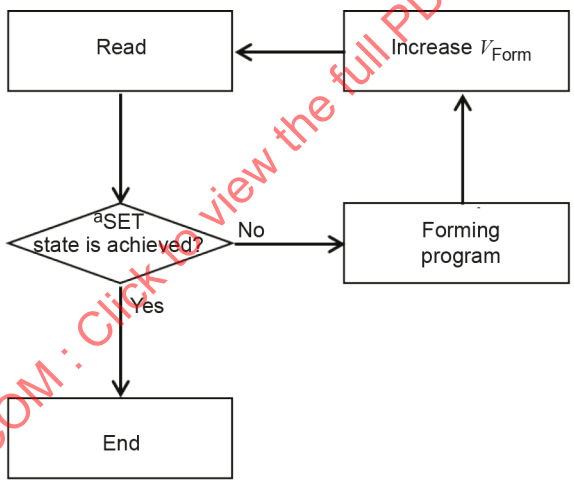


Figure 6 – Simulation test flow chart of the forming process

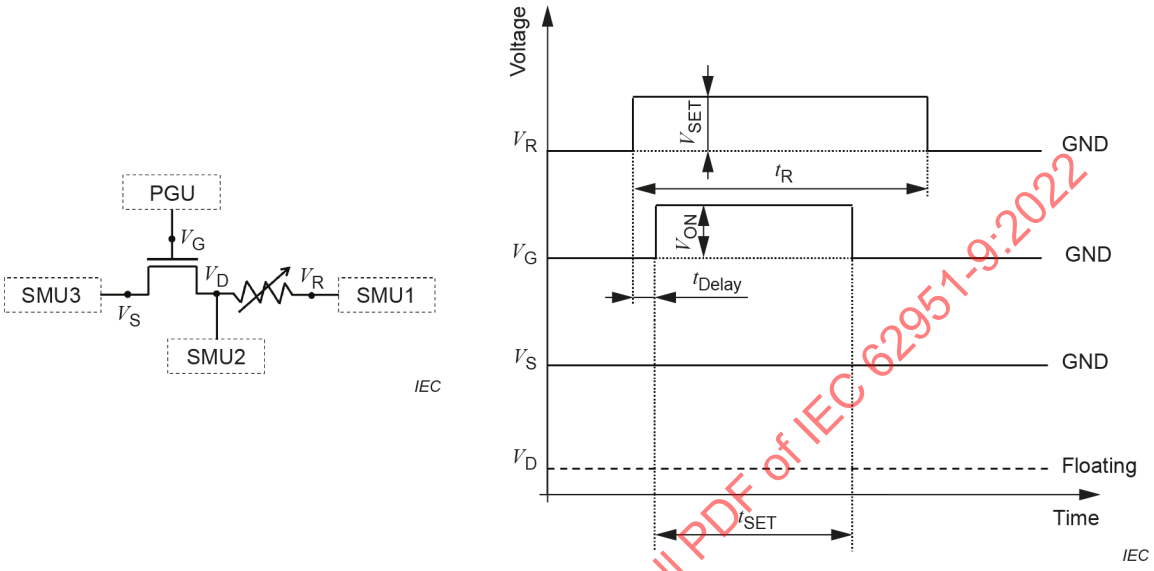
5.2.4 SET programming

Figure 7 a) shows the circuit diagram and Figure 7 b) shows the voltage-time graph to exhibit the SET operation of 1T1R resistive memory cell. 1T1R resistive memory cell (DUT) is programmed with V_S grounded and V_R applied to the TE of the resistive memory. For SET operation, V_{SET} is applied across the resistive memory having pulse width t_R and gate is biased with V_{ON} of pulse width t_{SET} to obtain the R_{LRS}.

$$t_{SET} < t_R$$

For the stable SET operation of the DUT, voltage ramp across the gate V_G is applied after some time span t_{Delay} as shown in Figure 7.

The simulation test flow chart in Figure 8 shows that before SET operation, the resistance state of the device is read; if it's in the R_{HRS}, the SET operation is initiated by applying the voltage V_{SET} to the TE of the resistive memory to achieve the SET state.



a) Circuit diagram **b) Voltage-time graph**

Figure 7 – SET operation of 1T1R resistive memory cell

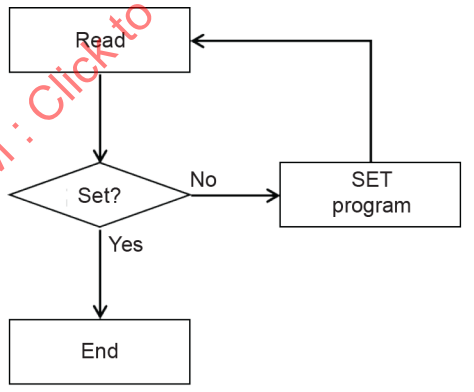


Figure 8 – Simulation test flow chart of the SET operation of 1T1R resistive memory cell

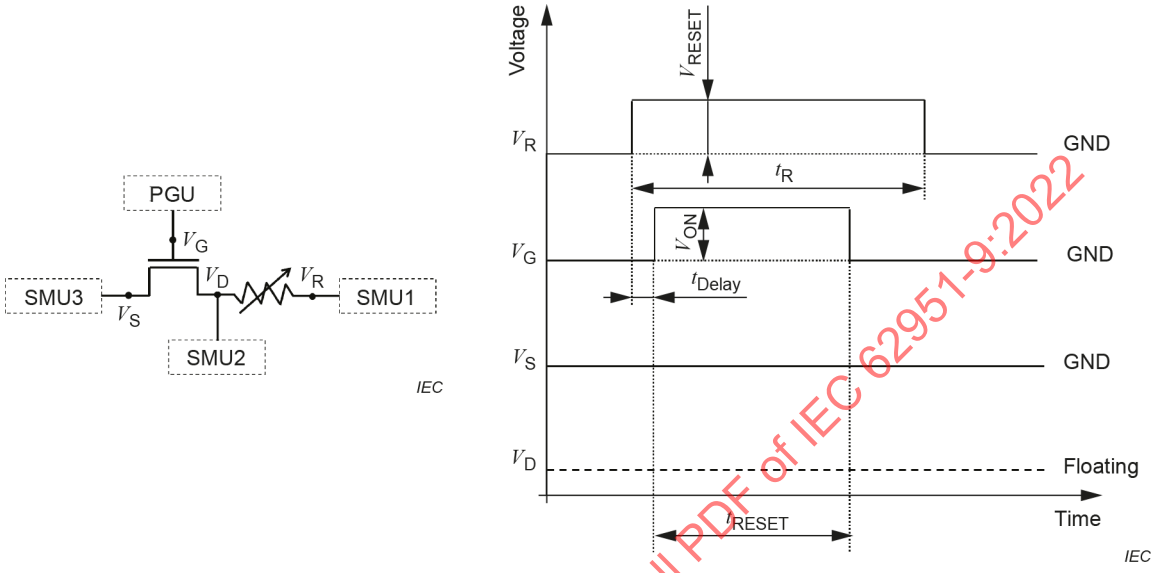
5.2.5 RESET programming

Figure 9 a) shows the circuit diagram and Figure 9 b) shows the voltage-time graph to exhibit the RESET operation of 1T1R resistive memory cell. For RESET operation, V_{RESET} is applied across the resistive memory having pulse width t_R and gate is biased with V_{ON} of pulse width t_{RESET} to obtain the R_{HRS}.

$$t_{RESET} < t_R$$

For the stable RESET operation of the DUT, voltage ramp across the gate V_G is applied after some time span t_{Delay} as shown in Figure 9.

The simulation test flow chart in Figure 10 shows that before RESET operation, the resistance state of the device is read; if it's already in the R_{LRS}, the RESET operation is initiated by applying the voltage V_{RESET} to the TE of the resistive memory to achieve the RESET state.



a) Circuit diagram **b) Voltage-time graph**

Figure 9 – RESET operation of 1T1R resistive memory cell

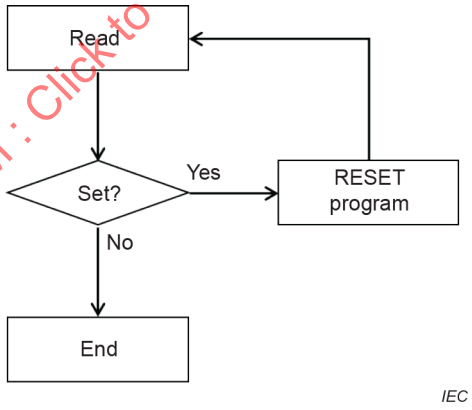


Figure 10 – Simulation test flow chart of the RESET operation of 1T1R resistive memory cell

Figure 11 shows the exemplary cumulative resistance distribution after the SET and RESET programming of 1T1R resistive memory.

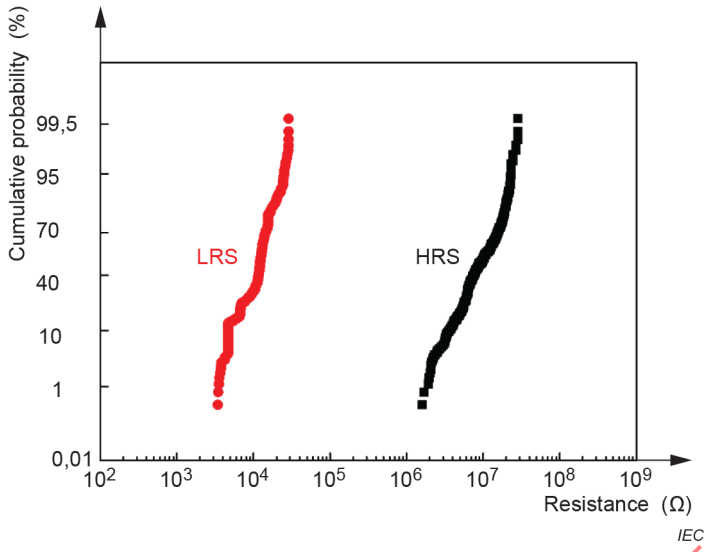


Figure 11 – Cumulative resistance distribution of 1T1R resistive memory

5.2.6 Endurance

Resistive memory can be switched between R_{HRS} and R_{LRS}, but each operation can introduce permanent damage, normally referred to as degradation. Endurance, also called electric fatigue, is the number of set/reset cycles that can be endured before HRS and LRS are no longer distinguishable, capability of the memory cell to reproduce its high and low resistance state over a course of continuous pulses typically until 10^6 cycles.

Memory devices are programmed by the application of voltage pulses. The characteristics of the applied pulses (e.g. pulse amplitude, pulse width, rise/fall times, etc.) depend on the test devices. (e.g. the oxide material, electrodes materials, active layer thicknesses, etc.). The programming pulses are controlled by PGU that can send and control the pulses. After every programming pulse, a read operation is performed. The current flowing through the memory cell is measured at several points during the read pulse. The resistance is then calculated using Ohm's law by averaging all the current measurements that have been acquired. If SET or RESET state of the device remains on applying the reverse operation for 3 consecutive pulses, the cycling endurance operation is adjourned. To be considered as an application for the field case, endurance in Figure 13 should be equal to or greater than 10^3.

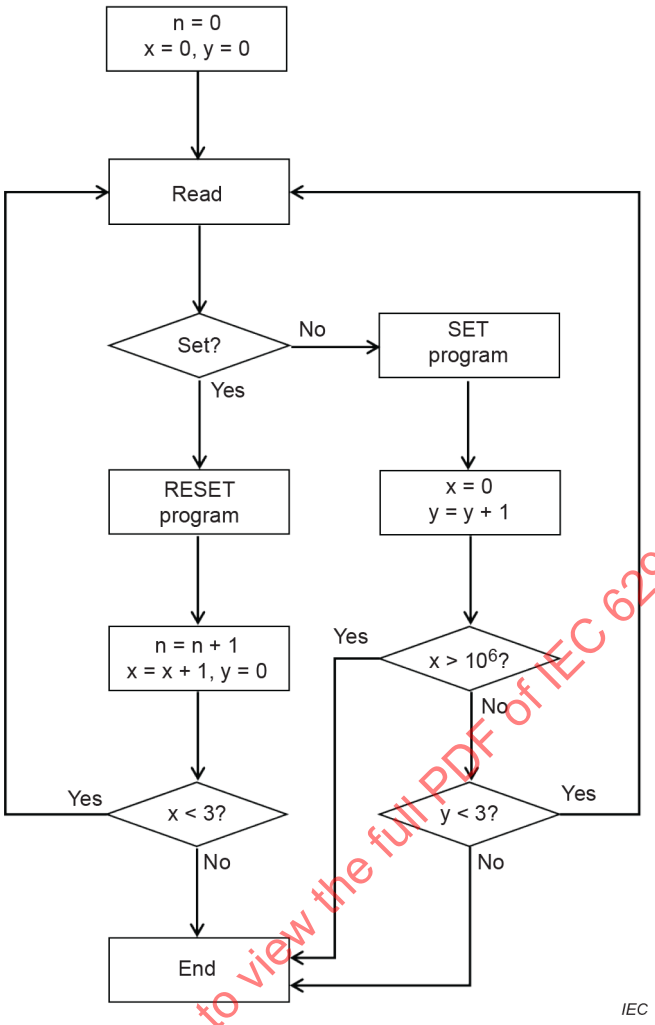


Figure 12 – Simulation test flow chart of the endurance test of 1T1R resistive memory cell

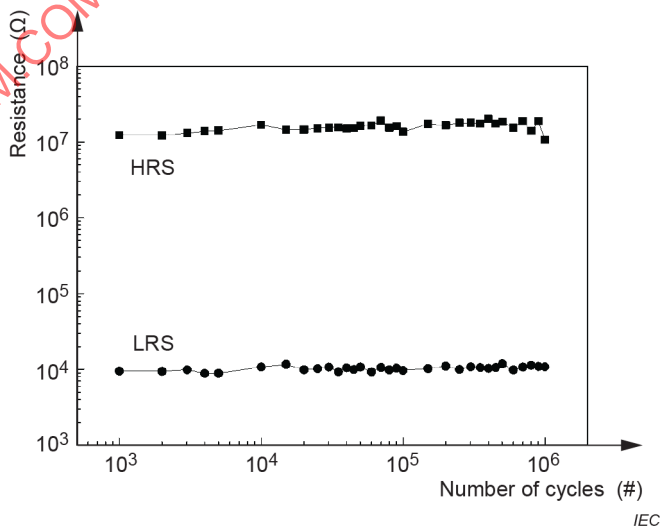


Figure 13 – Exemplary endurance data of a 1T1R resistive memory cell