

# INTERNATIONAL STANDARD

**Ferrite cores – Guidelines on dimensions and the limits of surface  
irregularities –  
Part 7: EER-cores**

IECNORM.COM : Click to view the full PDF of IEC 63093-7:2018





## THIS PUBLICATION IS COPYRIGHT PROTECTED

Copyright © 2018 IEC, Geneva, Switzerland

All rights reserved. Unless otherwise specified, no part of this publication may be reproduced or utilized in any form or by any means, electronic or mechanical, including photocopying and microfilm, without permission in writing from either IEC or IEC's member National Committee in the country of the requester. If you have any questions about IEC copyright or have an enquiry about obtaining additional rights to this publication, please contact the address below or your local IEC member National Committee for further information.

IEC Central Office  
3, rue de Varembé  
CH-1211 Geneva 20  
Switzerland

Tel.: +41 22 919 02 11  
[info@iec.ch](mailto:info@iec.ch)  
[www.iec.ch](http://www.iec.ch)

### About the IEC

The International Electrotechnical Commission (IEC) is the leading global organization that prepares and publishes International Standards for all electrical, electronic and related technologies.

### About IEC publications

The technical content of IEC publications is kept under constant review by the IEC. Please make sure that you have the latest edition, a corrigenda or an amendment might have been published.

#### IEC Catalogue - [webstore.iec.ch/catalogue](http://webstore.iec.ch/catalogue)

The stand-alone application for consulting the entire bibliographical information on IEC International Standards, Technical Specifications, Technical Reports and other documents. Available for PC, Mac OS, Android Tablets and iPad.

#### IEC publications search - [webstore.iec.ch/advsearchform](http://webstore.iec.ch/advsearchform)

The advanced search enables to find IEC publications by a variety of criteria (reference number, text, technical committee,...). It also gives information on projects, replaced and withdrawn publications.

#### IEC Just Published - [webstore.iec.ch/justpublished](http://webstore.iec.ch/justpublished)

Stay up to date on all new IEC publications. Just Published details all new publications released. Available online and also once a month by email.

#### Electropedia - [www.electropedia.org](http://www.electropedia.org)

The world's leading online dictionary of electronic and electrical terms containing 21 000 terms and definitions in English and French, with equivalent terms in 16 additional languages. Also known as the International Electrotechnical Vocabulary (IEV) online.

#### IEC Glossary - [std.iec.ch/glossary](http://std.iec.ch/glossary)

67 000 electrotechnical terminology entries in English and French extracted from the Terms and Definitions clause of IEC publications issued since 2002. Some entries have been collected from earlier publications of IEC TC 37, 77, 86 and CISPR.

#### IEC Customer Service Centre - [webstore.iec.ch/csc](http://webstore.iec.ch/csc)

If you wish to give us your feedback on this publication or need further assistance, please contact the Customer Service Centre: [sales@iec.ch](mailto:sales@iec.ch).



IEC 63093-7

Edition 1.0 2018-03

# INTERNATIONAL STANDARD

**Ferrite cores – Guidelines on dimensions and the limits of surface  
irregularities –  
Part 7: EER-cores**

IECNORM.COM : Click to view the full PDF of IEC 63093-7:2018

INTERNATIONAL  
ELECTROTECHNICAL  
COMMISSION

ICS 29.100.10

ISBN 978-2-8322-5485-1

**Warning! Make sure that you obtained this publication from an authorized distributor.**

## CONTENTS

FOREWORD .....	4
1 Scope .....	6
2 Normative references .....	6
3 Terms and definitions .....	6
4 Primary dimensions .....	6
4.1 General .....	6
4.2 Dimensions of EER-cores .....	7
4.2.1 Principal dimensions .....	7
4.2.2 Effective parameter and $A_{min}$ values .....	8
4.3 Dimensional limits for coil formers .....	8
5 Limits of surface irregularities .....	9
5.1 General .....	9
5.2 Chips and ragged edges .....	10
5.2.1 General .....	10
5.2.2 Chips and ragged edges on the mating surfaces (see Figure 4) .....	10
5.2.3 Chips and ragged edges on the other surfaces (see Figure 4) .....	10
5.3 Cracks .....	12
5.4 Flash .....	12
5.5 Pull-outs .....	12
5.6 Crystallites .....	13
5.7 Pores .....	14
Annex A (normative) Derived standards .....	15
Annex B (normative) Example of dimensions for gauges to check the dimensions of EER-cores meeting this primary standard .....	16
B.1 General .....	16
B.2 Procedure and requirements .....	16
Annex C (informative) Examples of allowable areas of chips .....	17
Bibliography .....	18
 Figure 1 – Dimensions of EER-cores .....	7
Figure 2 – Essential dimensions of coil formers .....	8
Figure 3 – Examples of surface irregularities .....	9
Figure 4 – Chip locations for EER-cores .....	10
Figure 5 – Cracks and pull-out locations for EER-cores .....	12
Figure 6 – Crystallite location for EER-cores .....	13
Figure 7 – Pore location for EER-cores .....	14
Figure B.1 – Gauge dimensions .....	16
 Table 1 – Dimensions of EER-cores .....	7
Table 2 – Effective parameter values of EER-cores .....	8

Table 3 – Dimensional limits for coil formers .....	9
Table 4 – Area and length reference for visual inspection .....	11
Table 5 – Limits for cracks .....	13
Table B.1 – Gauge dimensions .....	16
Table C.1 – Allowable areas of chips for EER-cores .....	17

IECNORM.COM : Click to view the full PDF of IEC 63093-7:2018

## INTERNATIONAL ELECTROTECHNICAL COMMISSION

---

**FERRITE CORES – GUIDELINES ON DIMENSIONS AND  
THE LIMITS OF SURFACE IRREGULARITIES –****Part 7: EER-cores****FOREWORD**

1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as "IEC Publication(s)"). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.

2) The formal decisions or agreements of IEC on technical matters express, as nearly as possible, an international consensus of opinion on the relevant subjects since each technical committee has representation from all interested IEC National Committees.

3) IEC Publications have the form of recommendations for international use and are accepted by IEC National Committees in that sense. While all reasonable efforts are made to ensure that the technical content of IEC Publications is accurate, IEC cannot be held responsible for the way in which they are used or for any misinterpretation by any end user.

4) In order to promote international uniformity, IEC National Committees undertake to apply IEC Publications transparently to the maximum extent possible in their national and regional publications. Any divergence between any IEC Publication and the corresponding national or regional publication shall be clearly indicated in the latter.

5) IEC itself does not provide any attestation of conformity. Independent certification bodies provide conformity assessment services and, in some areas, access to IEC marks of conformity. IEC is not responsible for any services carried out by independent certification bodies.

6) All users should ensure that they have the latest edition of this publication.

7) No liability shall attach to IEC or its directors, employees, servants or agents including individual experts and members of its technical committees and IEC National Committees for any personal injury, property damage or other damage of any nature whatsoever, whether direct or indirect, or for costs (including legal fees) and expenses arising out of the publication, use of, or reliance upon, this IEC Publication or any other IEC Publications.

8) Attention is drawn to the Normative references cited in this publication. Use of the referenced publications is indispensable for the correct application of this publication.

9) Attention is drawn to the possibility that some of the elements of this IEC Publication may be the subject of patent rights. IEC shall not be held responsible for identifying any or all such patent rights.

International Standard IEC 63093-7 has been prepared by IEC technical committee 51: Magnetic components, ferrite and magnetic powder materials.

This first edition cancels and replaces the first edition of IEC 62317-7 published in 2005. This edition constitutes a technical revision. This edition includes the following significant technical changes with respect to IEC 62317-7:

- IEC 63093-7 integrates IEC 62317-7 and IEC 60424-3;
- IEC 60424-3:2015, Table 2, has been included in Annex C as Table C.1.

The text of this International Standard is based on the following documents:

FDIS	Report on voting
51/1217/FDIS	51/1226/RVD

Full information on the voting for the approval of this International Standard can be found in the report on voting indicated in the above table.

This document has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 63093 series, published under the general title *Ferrite cores – Guidelines on dimensions and the limits of surface irregularities* can be found on the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under "<http://webstore.iec.ch>" in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

A bilingual version of this publication may be issued at a later date.

IECNORM.COM : Click to view the full PDF of IEC 63093-7:2018

## FERRITE CORES – GUIDELINES ON DIMENSIONS AND THE LIMITS OF SURFACE IRREGULARITIES –

### Part 7: EER-cores

#### 1 Scope

This part of IEC 63093 specifies the dimensions that are of importance for mechanical interchangeability for a preferred range of EER-cores made of ferrite, the essential dimensions of coil formers to be used with them as well the effective parameter values to be used in calculations involving them, and gives guidelines on allowable limits of surface irregularities applicable to EER-cores.

This document is a specification useful in the negotiations between ferrite core manufacturers and customers about surface irregularities.

The use of “derived” standards which give more detailed specifications of component parts while still permitting compliance with this document is discussed in Annex A.

#### 2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60205, *Calculation of the effective parameters of magnetic piece parts*

IEC 60401-1, *Terms and nomenclature for cores made of magnetically soft ferrites – Part 1: Terms used for physical irregularities*

IEC 60424-1, *Ferrite cores – Guidelines on the limits of surface irregularities – Part 1: General specification*

#### 3 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 60401-1 and IEC 60424-1 apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at <http://www.electropedia.org/>
- ISO Online browsing platform: available at <http://www.iso.org/obp>

#### 4 Primary dimensions

##### 4.1 General

Compliance with the following requirements ensures mechanical interchangeability of complete assemblies and coil formers.

## 4.2 Dimensions of EER-cores

### 4.2.1 Principal dimensions

The principal dimensions of EER-cores shall be those given in Table 1. The dimensions of the cores may be checked by means of gauges. By way of example, possible dimensions for these gauges are given in Annex B. In order to facilitate production, it may be necessary to use gauges having dimensions that differ from those given in Annex B, although no relaxation of the requirements for the dimensions of the cores given in Table 1 is permitted. The dimensions specified in Table 1 are illustrated in Figure 1.

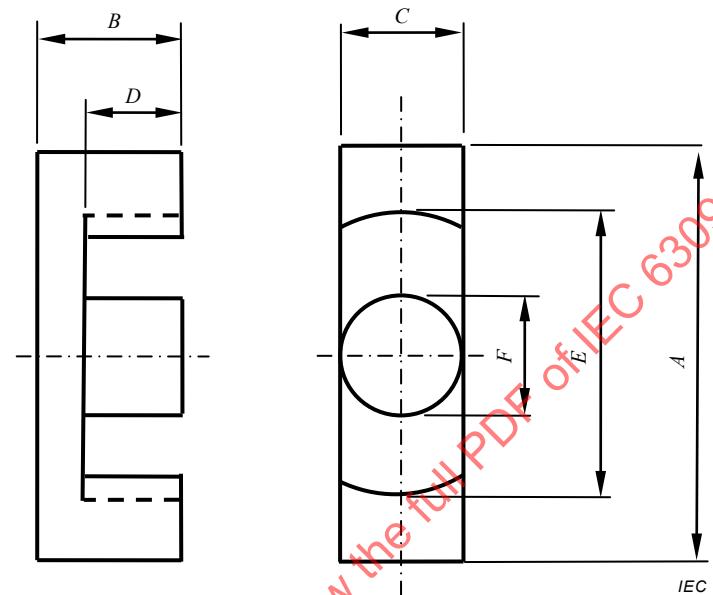


Figure 1 – Dimensions of EER-cores

Table 1 – Dimensions of EER-cores

Size	A mm		B mm		C mm		D mm		E mm		F mm	
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
EER25,5	24,9	26,1	9,05	9,55	7,25	7,75	5,95	6,45	19,7	20,9	7,25	7,75
EER28	27,9	29,1	13,7	14,3	11,1	11,7	9,3	9,9	21,1	22,3	9,6	10,2
EER28L	27,9	29,1	16,6	17,2	11,1	11,7	12,2	12,8	21,1	22,3	9,6	10,2
EER35	34,2	35,8	20,4	21,0	11,0	11,6	14,4	15,0	25,3	26,9	11,0	11,6
EER39	38,2	39,8	21,8	22,6	12,5	13,1	16,6	17,4	28,4	30,0	12,5	13,1
EER40	39,5	40,5	22,2	22,6	13,05	13,55	15,1	15,7	29,0	30,8	13,05	13,55
EER42	41,1	42,9	20,8	21,6	14,8	15,6	14,9	15,7	29,2	31,0	14,8	15,6
EER49	47,9	50,1	30,8	31,6	16,8	17,6	22,3	23,1	36,0	38,2	16,8	17,6

#### 4.2.2 Effective parameter and $A_{\min}$ values

The effective parameter values of a pair of cores whose dimensions comply with 4.2.1 shall be as given in Table 2. For the definitions of these parameters and their calculations, see IEC 60205.

**Table 2 – Effective parameter values of EER-cores**

Size	$C_1$ mm <sup>-1</sup>	$C_2$ mm <sup>-3</sup>	$l_e$ mm	$A_e$ mm <sup>2</sup>	$V_e$ mm <sup>3</sup>	$A_{\min}^a$ mm <sup>2</sup>
EER25,5	1,070 0	$2,408\ 7 \times 10^{-2}$	47,5	44,4	2 110	42,5
EER28	0,728 16	$0,843\ 36 \times 10^{-2}$	62,9	86,4	5 430	77,0
EER28L	0,868 36	$1,013\ 8 \times 10^{-2}$	74,4	85,7	6 370	77,0
EER35	0,815 66	$0,738\ 15 \times 10^{-2}$	90,1	111	9 960	100
EER39	0,762 91	$0,573\ 84 \times 10^{-2}$	101	133	13 500	129
EER40	0,643 21	$0,424\ 31 \times 10^{-2}$	97,5	152	14 800	139
EER42	0,510 64	$0,272\ 52 \times 10^{-2}$	95,7	187	17 900	179
EER49	0,557 95	$0,231\ 33 \times 10^{-2}$	134	241	32 400	228

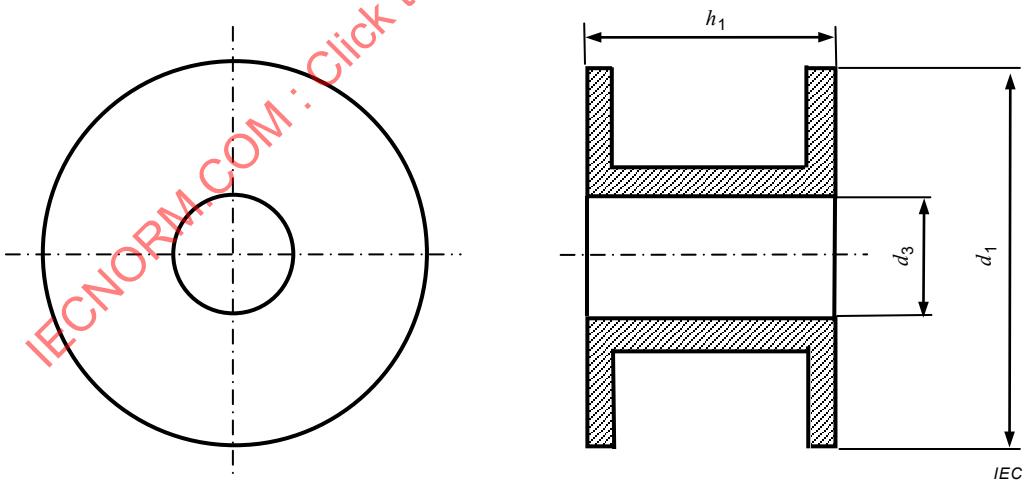
NOTE 1 The manufacturers can indicate in their catalogues more precise values than those given in Table 2.

NOTE 2 The above values have been calculated using the method given in IEC 60205.

<sup>a</sup> See IEC 60205 for the definition of  $A_{\min}$ .

#### 4.3 Dimensional limits for coil formers

The essential dimensions of coil formers suitable for use with a pair of EER-cores shall be as given in Table 3. The dimensions specified in Table 3 are illustrated in Figure 2.



**Figure 2 – Essential dimensions of coil formers**

**Table 3 – Dimensional limits for coil formers**

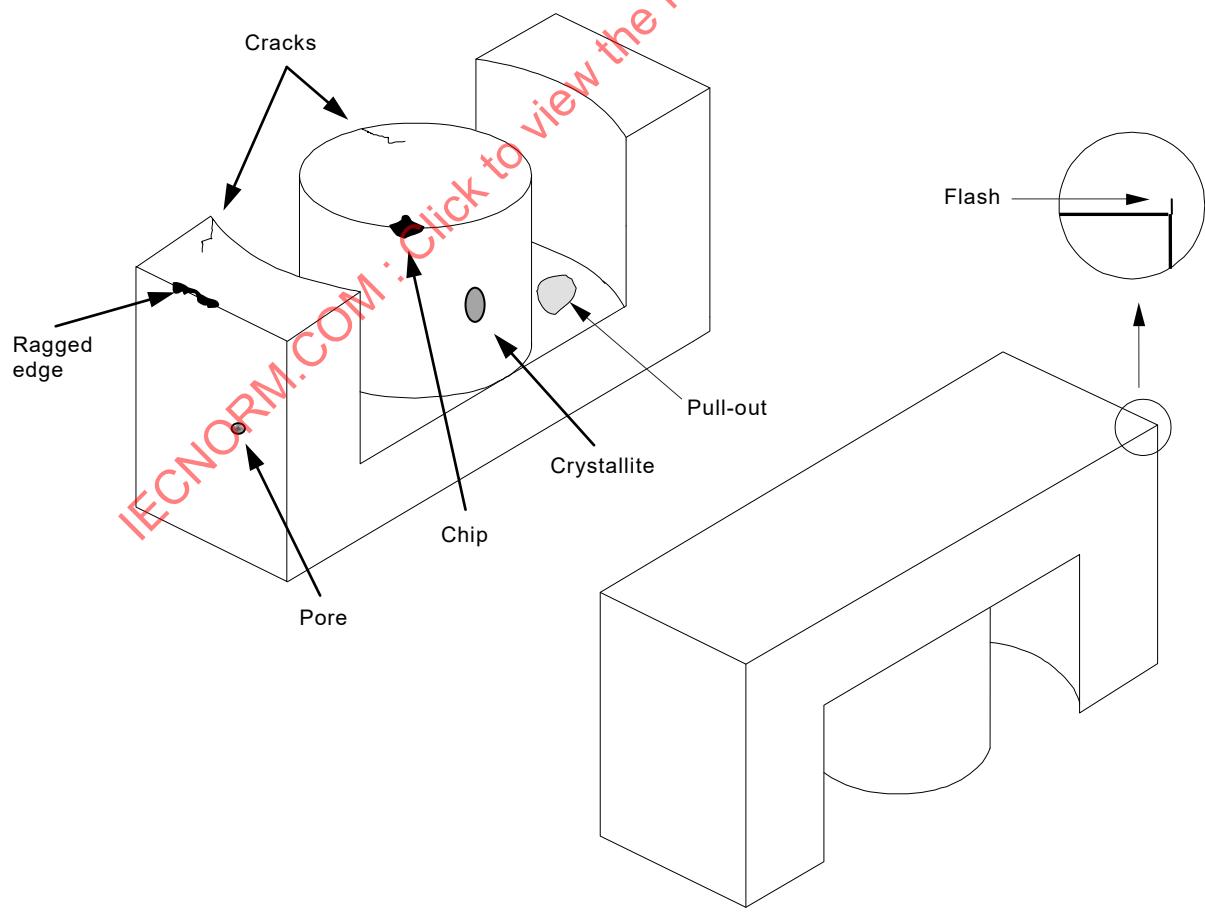
Size	$d_1$ mm	$d_3$ mm	$h_1$ mm
	Max.	Min.	Max.
EER 25,5	19,3	8,0	11,7
EER 28	20,7	10,4	18,4
EER 28L	20,7	10,4	24,2
EER 35	24,9	11,8	28,6
EER 39	27,9	13,3	33,0
EER 40	28,5	13,8	30,0
EER 42	28,6	15,8	29,6
EER 49	35,4	17,9	44,3

## 5 Limits of surface irregularities

### 5.1 General

Surface irregularities are defined in IEC 60424-1.

Figure 3 shows different examples of surface irregularities of an EER-core.

**Figure 3 – Examples of surface irregularities**

## 5.2 Chips and ragged edges

### 5.2.1 General

The minimum area is taken as  $0,5 \text{ mm}^2$ , to be distinguishable to the naked eye.

### 5.2.2 Chips and ragged edges on the mating surfaces (see Figure 4)

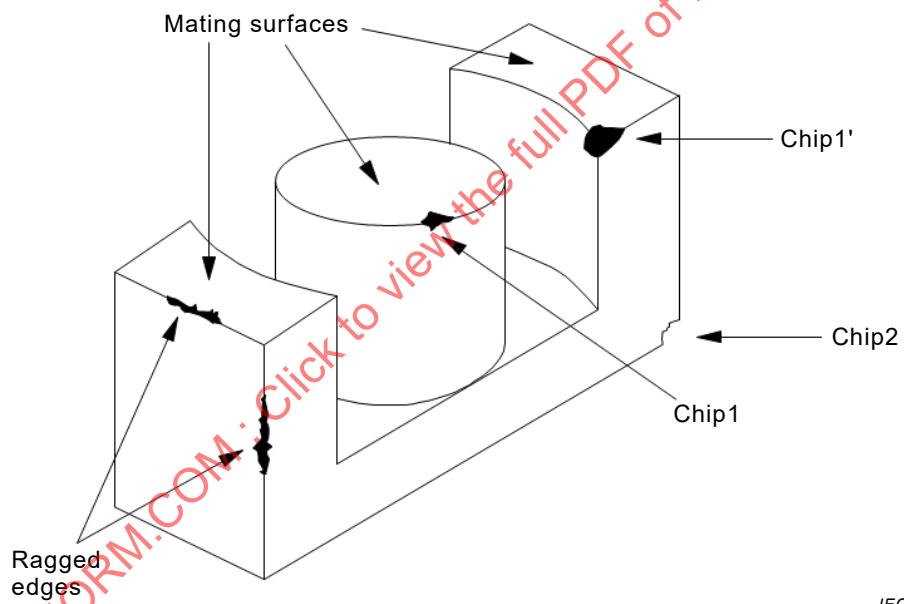
The areas of the chips located on the mating surfaces (chip1 and chip1' irregularities of Figure 4) shall not exceed the following limits:

- the cumulative area of the chips shall be less than 6 % of the mating surface (whether gapped or ungapped) of the centre pole;
- the total length of the ragged edges shall be less than 25 % of the perimeter of the relevant surface.

### 5.2.3 Chips and ragged edges on the other surfaces (see Figure 4)

The allowable areas of chips are doubled as compared to the limits for the mating surfaces.

The rule for ragged edges is the same as that for the mating surfaces.



IEC

**Figure 4 – Chip locations for EER-cores**

Area and length reference for visual inspection is given in Table 4. Examples of allowable areas of chips are given in Annex C.

**Table 4 – Area and length reference for visual inspection**

Area	A	B	C	D	E	Area	A	B	C	D	E
0,5 mm <sup>2</sup>	•	▪	-	-	▼	12,5 mm <sup>2</sup>	●	■	■	—	▲
1,0 mm <sup>2</sup>	•	▪	-	-	▼	15,0 mm <sup>2</sup>	●	■	■	—	▲
1,5 mm <sup>2</sup>	•	▪	-	-	▼	17,5 mm <sup>2</sup>	●	■	■	—	▲
2,0 mm <sup>2</sup>	•	▪	-	-	▼	20,0 mm <sup>2</sup>	●	■	■	—	▲
2,5 mm <sup>2</sup>	•	▪	-	-	▼	25,0 mm <sup>2</sup>	●	■	—	—	▲
3,0 mm <sup>2</sup>	•	▪	-	-	▼	30,0 mm <sup>2</sup>	●	■	—	—	▲
3,5 mm <sup>2</sup>	•	▪	-	-	▼	35,0 mm <sup>2</sup>	●	■	—	—	▲
4,0 mm <sup>2</sup>	•	▪	-	-	▼	40,0 mm <sup>2</sup>	●	■	—	—	▲
4,5 mm <sup>2</sup>	•	▪	-	-	▼	45,0 mm <sup>2</sup>	●	■	—	—	▲
5,0 mm <sup>2</sup>	•	▪	-	-	▼	50,0 mm <sup>2</sup>	●	■	—	—	▲
6,0 mm <sup>2</sup>	●	■	■	—	▼						
7,0 mm <sup>2</sup>	●	■	■	—	▼						
8,0 mm <sup>2</sup>	●	■	■	—	▼						
9,0 mm <sup>2</sup>	●	■	■	—	▼						
10,0 mm <sup>2</sup>	●	■	■	—	▼						

Scale 1:1

1 mm —      2 mm —      3 mm —      4 mm —  
 5 mm —      7,5 mm —      10 mm —

IEC

### 5.3 Cracks

The limits for cracks at various locations shown in Figure 5 are given in Table 5.

### 5.4 Flash

There shall be no flash extending from the core into the wire-slot (see Figure 5).

### 5.5 Pull-outs

For EER-cores, the cumulative area of pull-outs of the core shall be less than 25 % of the total respective surface area (see Figure 5).

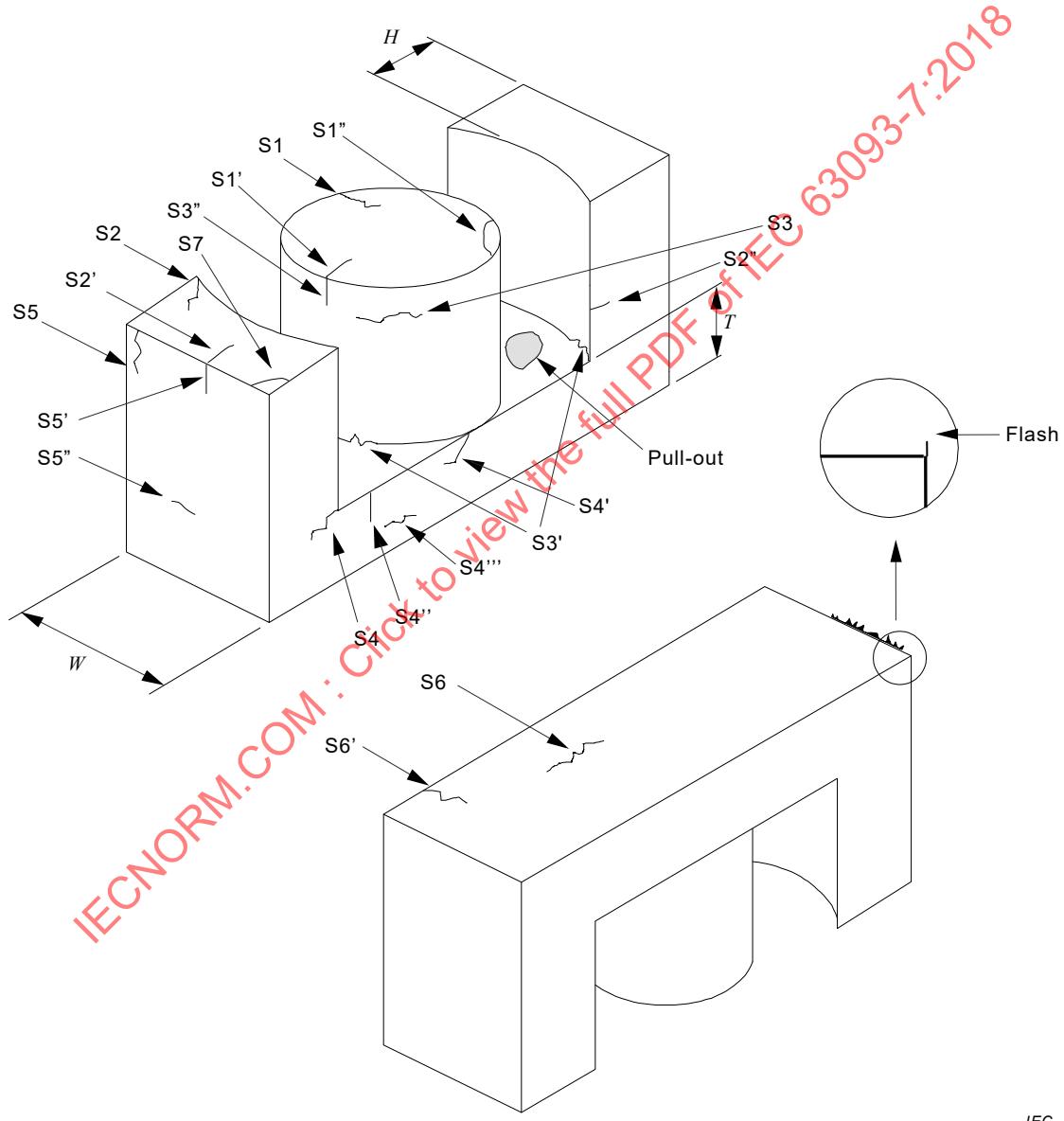


Figure 5 – Cracks and pull-out locations for EER-cores

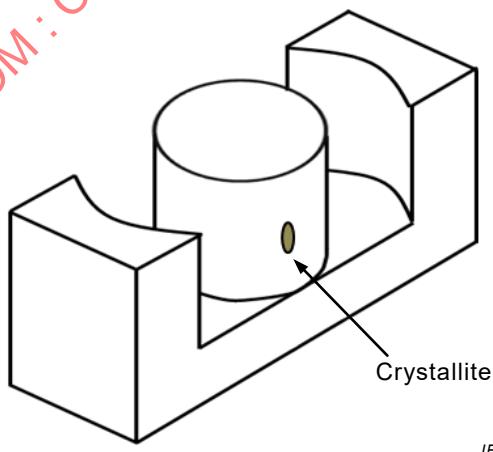
**Table 5 – Limits for cracks**

Type	Location	Limits for single crack	Limits for multiple cracks
S1 and S1'	Mating surface of centre pole	< 25 % of dimension $W$	< 50 % of dimension $W$
S1"	Corner of centre pole	Not acceptable	Not acceptable
S2 and S2'	Mating surface of outer leg	< 25 % of dimension $H$	< 25 % of dimension $H$
S2"	Side of outer leg	< 25 % of dimension $H$	< 25 % of dimension $H$
S3 and S3"	Centre pole	< 25 % of dimension $W$	< 25 % of dimension $W$
S3'	Bottom corner of centre pole/back wall and outer leg/back wall	< 25 % of dimension $W$	< 25 % of dimension $W$
S4	Bottom corner of outer leg/back wall	< 25 % of dimension $T$	< 25 % of dimension $T$
S4' and S4"	Back wall	< 25 % of dimension $T$	< 25 % of dimension $T$
S4'''	Back wall	< 50 % of dimension $W$	< 100 % of dimension $W$
S5, S5' and S5"	Outer leg	< 50 % of dimension $W$	< 100 % of dimension $W$
S6	Back surface	< 50 % of dimension $W$	< 100 % of dimension $W$
S6'	Back surface	< 25 % of dimension $W$	< 25 % of dimension $W$
S7	Corner of outer leg	Not acceptable	Not acceptable

## 5.6 Crystallites

Figure 6 shows an example of crystallite location on EER-cores:

- A single area of crystallites located on any surface shall be less than 2 % of the respective surface area.
- The cumulative area of crystallites located on any surface shall be less than 4 % of the respective surface area (see Figure 6).



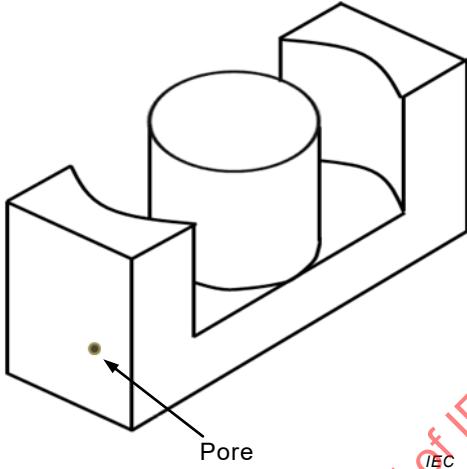
IEC

**Figure 6 – Crystallite location for EER-cores**

## 5.7 Pores

Figure 7 shows an example of pore location on EER cores:

- The number of pores located on the same surface shall not exceed two. The total number of pores located on all surfaces shall not exceed five.
- A hole with an area larger than  $1 \text{ mm}^2$  on any surface is not acceptable.



**Figure 7 – Pore location for EER-cores**

**Annex A**  
(normative)**Derived standards**

Clauses 1 to 4 of this document establish the values for the principal dimensions of core assemblies and coil formers and enable full interchangeability for components complying with this primary standard to be achieved.

Parties interested in making or using EER-cores may find it desirable to lay down local standards for everyday use, which show the dimensions and tolerances in greater detail than Clause 4, and which correspond to the state of the art in that area. These specifications are known as “derived standards”. When doing so, care should be taken not to exclude any other type of EER-core meeting this primary standard, which would also satisfy the performance specification valid for a specific case.

It should be noted that even if a component complies with a derived standard and with the requirements of Clause 4 of this primary standard, therefore permitting core assemblies and coil formers to be freely interchanged, its constituent parts may not necessarily be interchangeable.

When requirements lead to the establishment of a national standard, the relevant national standardization body is strongly requested to insert a note in such a national standard stating that:

- a) it is in accordance with the dimensional requirements of this present primary standard but that more details are given in order to promote its practical use;
- b) other solutions are possible within the framework of this primary standard and should not be excluded if the resulting core and coil formers are functionally interchangeable with those of the national standard.