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Road vehicles — Media Oriented Systems Transport (MOST) —

Part 8: 150-Mbit/s optical physical layer

Véhicules routiers — Système de transport axé sur les médias —

Partie 8: Couche optique physique à150-Mbit/s

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Foreword

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This document was prepared by Technical Committee ISO/TC 22, *Road vehicles*, Subcommittee SC 31, *Data communication*.

A list of all parts in the ISO 21806 series can be found on the ISO website.

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Introduction

The Media Oriented Systems Transport (MOST) communication technology was initially developed at the end of the 1990s in order to support complex audio applications in cars. The MOST Cooperation was founded in 1998 with the goal to develop and enable the technology for the automotive industry. Today, MOST[1)] enables the transport of high quality of service (QoS) audio and video together with packet data and real-time control to support modern automotive multimedia and similar applications. MOST is a function-oriented communication technology to network a variety of multimedia devices comprising one or more MOST nodes.

Figure 1 shows a MOST network example.

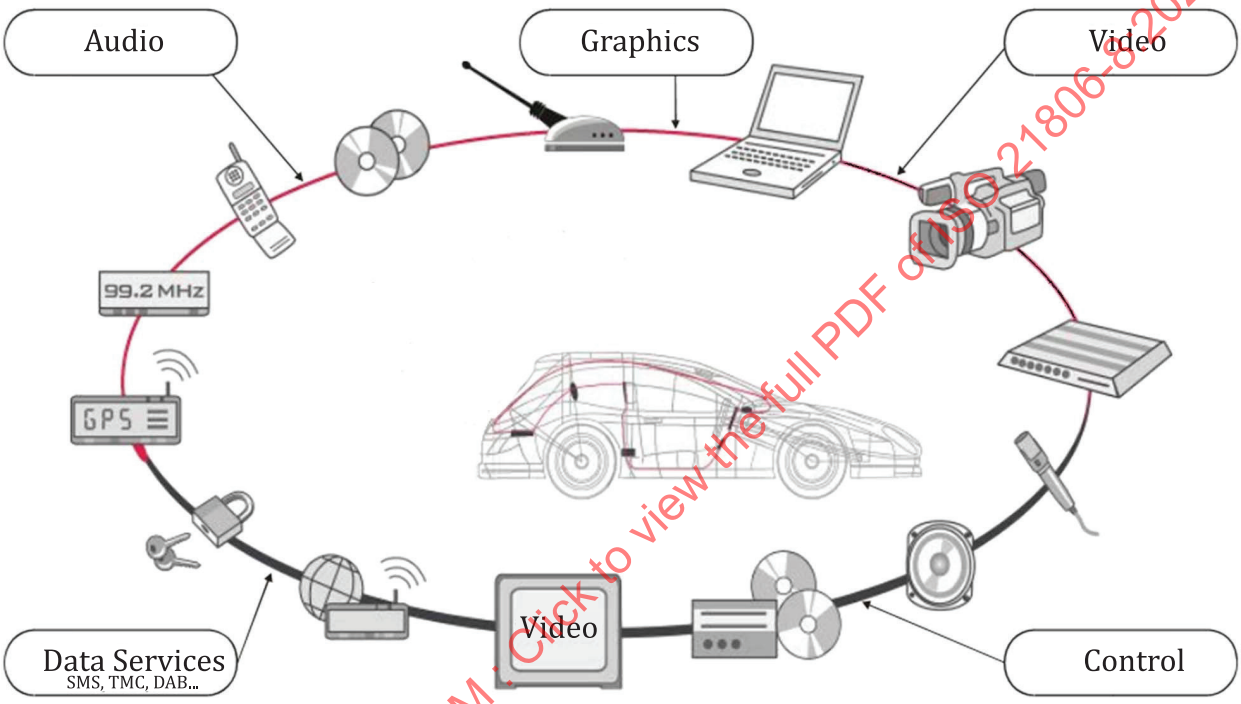

Figure 1 — MOST network example

The MOST communication technology provides:

— synchronous and isochronous streaming,

— small overhead for administrative communication control,

— a functional and hierarchical system model,

— API standardization through a function block (FBlock) framework,

— free partitioning of functionality to real devices,

— service discovery and notification, and

— flexibly scalable automotive-ready Ethernet communication according to ISO/IEC/IEEE 8802-3[4].

MOST is a synchronous time-division-multiplexing (TDM) network that transports different data types on separate channels at low latency. MOST supports different bit rates and physical layers. The network clock is provided with a continuous data signal.

1) MOST® is the registered trademark of Microchip Technology Inc. This information is given for the convenience of users of this document and does not constitute an endorsement by ISO.

Within the synchronous base data signal, the content of multiple streaming connections and control data is transported. For streaming data connections, bandwidth is reserved to avoid interruptions, collisions, or delays in the transport of the data stream.

MOST specifies mechanisms for sending anisochronous, packet-based data in addition to control data and streaming data. The transmission of packet-based data is separated from the transmission of control data and streaming data. None of them interfere with each other.

A MOST network consists of devices that are connected to one common control channel and packet channel.

In summary, MOST is a network that has mechanisms to transport the various signals and data streams that occur in multimedia and infotainment systems.

The ISO standards maintenance portal (https://standards.iso.org/iso/) provides references to MOST specifications implemented in today's road vehicles because easy access via hyperlinks to these specifications is necessary. It references documents that are normative or informative for the MOST versions 4V0, 3V1, 3V0, and 2V5.

The ISO 21806 series has been established in order to specify requirements and recommendations for implementing the MOST communication technology into multimedia devices and to provide conformance test plans for implementing related test tools and test procedures.

To achieve this, the ISO 21806 series is based on the open systems interconnection (OSI) basic reference model in accordance with ISO/IEC 7498-1[2] and ISO/IEC 10731[3], which structures communication systems into seven layers as shown in Figure 2. Stream transmission applications use a direct stream data interface (transparent) to the data link layer.

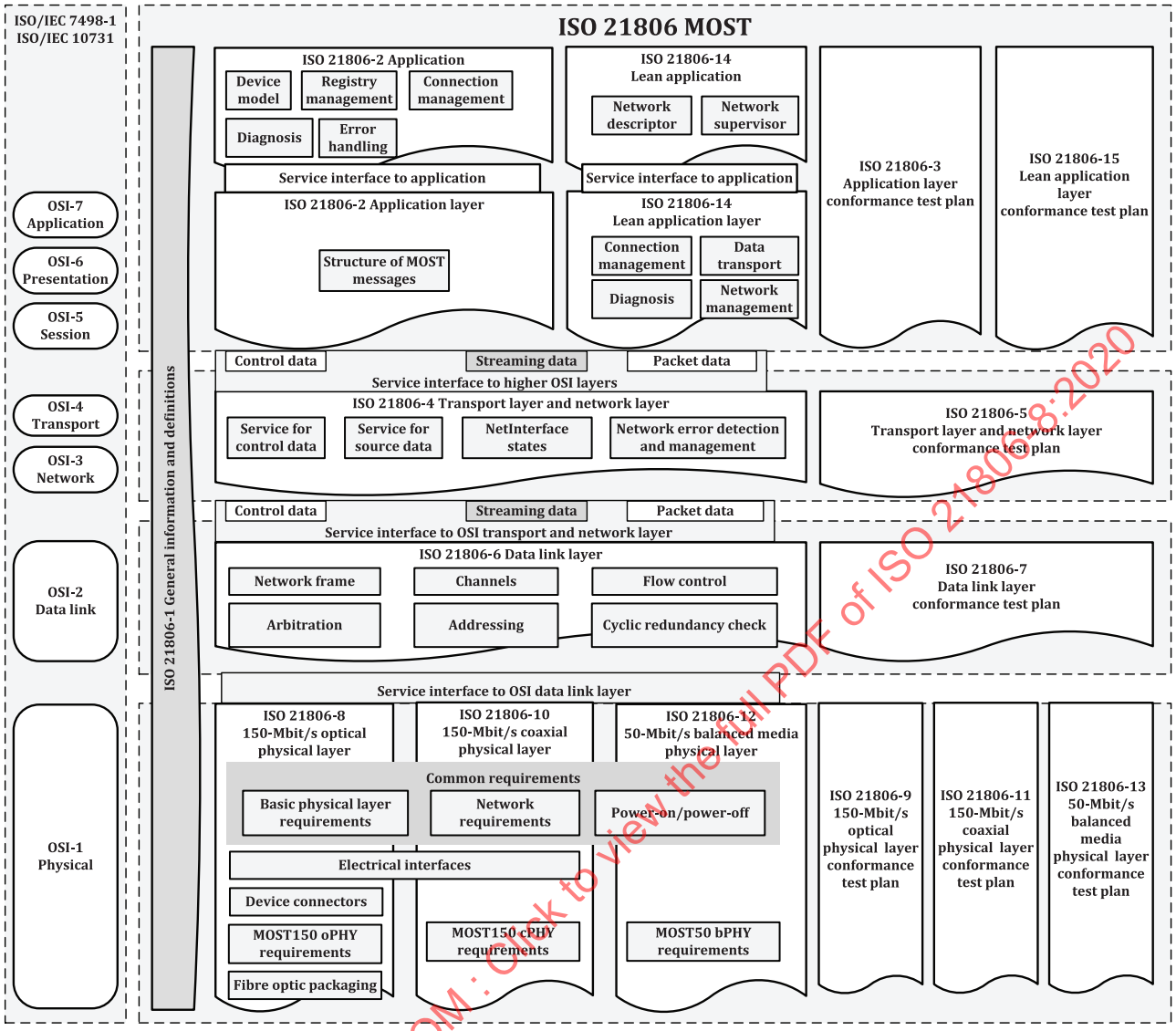

Figure 2 — The ISO 21806 series reference according to the OSI model

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Road vehicles — Media Oriented Systems Transport (MOST) —

Part 8: 150-Mbit/s optical physical layer

1 Scope

This document specifies the 150-Mbit/s optical physical layer for MOST (MOST150 oPHY), a synchronous time-division-multiplexing network.

This document specifies the applicable constraints and defines interfaces and parameters, suitable for the development of products based on MOST150 oPHY. Such products include fibre optical links and connectors, fibre optic receivers, fibre optic transmitters, electrical to optical converters, and optical to electrical converters.

This document also establishes basic measurement techniques and actual parameter values for MOST150 oPHY.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

ISO 21806-1, *Road vehicles — Media Oriented Systems Transport (MOST) — Part 1: General information and definitions*

IEC 60825-2, *Safety of laser products — Part 2: Safety of optical fibre communication systems (OFCS)*

JEDEC MS-013E[2], *Standard — Very Thick Profile, Plastic Small Outline (SO) Family, 1,27 mm pitch, 7,50 mm (.300 inch) Body Width*. R1B-PDSO/SOP/SOIC

JEDEC No. JESD8C.01[3], *Interface Standard for Nominal 3 V/3,3 V Supply Digital Integrated Circuits*

TIA/EIA-644-A[4], *Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits*

3 Terms and definitions

For the purposes of this document, the terms and definitions given in ISO 21806-1 and the following apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

— ISO Online browsing platform: available at https://www.iso.org/obp

— IEC Electropedia: available at http://www.electropedia.org/

2) Available at https://www.jedec.org/.

3) Available at https://www.jedec.org/.

4) Available at https://www.tiaonline.org/standards/.

3.1
electrical to optical converter
EOC
MOST component that converts an electrical signal into an optical signal

3.2
MOST150 oPHY
150-Mbit/s optical physical layer

3.3
numerical aperture
NA
sine of the vertex angle of the largest cone of meridional rays that can enter or leave an optical system or element, multiplied by the refractive index of the medium in which the vertex of the cone is located

[SOURCE: IEC Electropedia, 731-03-85]

3.4
optical to electrical converter
OEC
MOST component that converts an optical signal into an electrical signal

3.5
pigtail
short length of optical fibre, permanently attached to a component and intended to facilitate jointing between that component and another optical fibre or component

[SOURCE: IEC Electropedia, 731-05-08, modified — The term was originally "optical fibre pigtail" and the Note 1 to entry has been deleted.]

4 Symbols and abbreviated terms

4.1 Symbols

---	empty cell/undefined
b_0	the optical signal level when a logic 0 is transmitted
b_1	the optical signal level when a logic 1 is transmitted
N_{BPF}	bits per frame
ρ_{Fs}	network frame rate
ρ_{BR}	bit rate
T_A	ambient temperature
t_{MDT}	TimingMaster delay tolerance
t_{UI}	unit interval
V_{OH}	output high voltage
V_{OL}	output low voltage

4.2 Abbreviated terms

BER	bit error rate
BPF	bits per frame
Cd[n]	condition
DC	direct current
DCA	DC adaptive
DDJ	data-dependant jitter
DLL	data link layer
DSV	digital sum value
ECU	electronic control unit
EOC	electrical to optical converter
EMC	electromagnetic compatibility
EMI	electromagnetic interference
FOR	fibre optic receiver
FOT	fibre optic transceiver
FOX	fibre optic transmitter
LS	low sensitivity
LVDS	Low Voltage Differential Signaling
NA	numerical aperture
N/A	not applicable
MNC	MOST network controller
OEC	optical to electrical converter
oPHY	optical physical layer
PCB	printed circuit board
PDF	probability density function
PHY	physical layer
PLL	phase locked loop
POF	polymer (plastic) optical fibre
RMS	root mean square
Rx data	MOST150 oPHY automotive encoded digital bit stream being received
SDA	serial data analyser

SP[n]	Specification Point
TDM	time-division-multiplexing
Tx data	MOST150 oPHY automotive encoded digital bit stream being transmitted
UI	unit interval

5 Conventions

This document is based on OSI service conventions as specified in ISO/IEC 10731[3].

6 Physical layer service interface to OSI data link layer

6.1 Overview

The physical layer (PHY) service interface specifies the abstract interface to the OSI data link layer (DLL), see ISO 21806-6[1].

6.2 Data type definitions

The data type `Enum` is defined as an 8-bit enumeration.

6.3 Event indications and action requests

6.3.1 P_EVENT.INDICATE

The PHY shall use `P_EVENT.INDICATE` to indicate the occurrence of an event to the DLL.

```
P_EVENT.INDICATE{
    PHY_Event
}
```

6.3.2 P_ACTION.REQUEST

`P_ACTION.REQUEST` shall trigger the execution of a request.

```
P_ACTION.REQUEST {
    PHY_Request
}
```

6.4 Parameters

6.4.1 PHY_Event

Table 1 specifies the `PHY_Event` parameter, which notifies the DLL about events.

Table 1 — Parameter passed from PHY to DLL

Parameter	Data type	Description

PHY_Event	Enum {
	PHY_Output_Off,
	PHY_Network_Activity
	}
		An event that is reported to the DLL.

Table 2 specifies the parameter values for the PHY_Event Enum.

Table 2 — PHY_Event Enum values

Enum value	Description
PHY_Output_Off	MNC transmit terminal switched off.
PHY_Network_Activity	Network activity detected at the MNC receive terminal.

6.4.2 PHY_Request

Table 3 specifies the PHY_Request parameter, which is passed from DLL to PHY.

Table 3 — Parameter passed from DLL to PHY

Parameter	Data type	Description

PHY_Request	Enum {
	cmd_Output_Off,
	cmd_Output_On,
	cmd_Open_Bypass,
	}
		A request from the DLL

Table 4 specifies the parameter values for the PHY_Request Enum.

Table 4 — PHY_Request Enum values

Enum value	Description
cmd_Output_Off	Switching off the MNC transmit terminal requested. By default, it is off.
cmd_Output_On	Switching on the MNC transmit terminal requested. By default, it is off.
cmd_Open_Bypass	Opening the bypass requested. By default, the bypass is closed.

7 Basic physical layer requirements

7.1 Logic terminology

7.1.1 Single-ended low-voltage digital signals

For the parameters provided in JEDEC No. JESD8C.01, Table 5 defines the corresponding terms for single-ended signals used in this document. These terms are used to describe the logic states of signals /RST and STATUS.

Table 5 — Terms for single-ended signals

Term	Corresponding JEDEC parameter
Low	V_{OL} (output low voltage)
Logic 0	
High	V_{OH} (output high voltage)
Logic 1	

7.1.2 Differential LVDS signals

TIA/EIA-644-A uses the labels A and B for the device output terminals; this document uses P and an N, respectively. Table 6 specifies the terms for LVDS signals. The terms correspond to the TIA/EIA-644-A specification.

Table 6 — Terms for LVDS signals

Term	Corresponding JEDEC parameter
Low	The P terminal shall be negative with respect to the N terminal for a binary 0 state.
Logic 0	
High	The P terminal shall be positive with respect to the N terminal for a binary 1 state.
Logic 1	

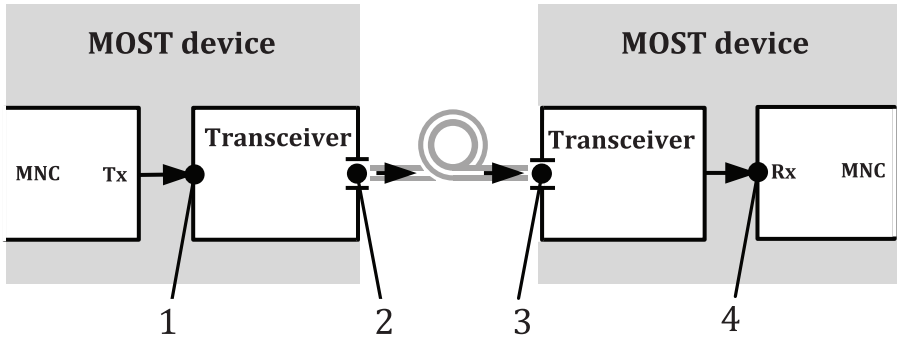
Since some of the MOST devices specified in this document use a tri-state LVDS interface, Table 7 specifies the terms for LVDS bus states.

Table 7 — Terms for LVDS bus states

Term	Corresponding TIA/EIA description
Disabled	The P and N terminals are in a high impedance state. If small leakage currents exist, they might cause an indeterminate voltage on the line/load.
Off	
Enabled	The P and the N terminals are driving the line/load. The outputs are at valid LVDS logic levels provided the input data is valid.
On	
Valid LVDS signal	Data or LVDS 0, according to LVDS voltage levels.

7.2 Specification points (SPs)

A physical connection of two MOST devices is called a link. Measurements are taken at specific locations along a link. These locations are called SPs. The location of the SPs is shown in Figure 3.



Key

1 specification point 1
2 specification point 2
3 specification point 3
4 specification point 4

Figure 3 — Location of SPs along a link

SPs define interfaces that are boundaries between a transmitting and a receiving MOST component. For each of those interfaces, a set of requirements and properties is defined (e.g. signal timing, signal amplitude, connector interface drawings). SP1 and SP4 are located between a MOST network controller (MNC) and the corresponding transceiver. SP2 and SP3 are located between transceivers and a wiring harness.

For MOST components that are located between two adjacent SPs, requirements and properties can be derived. The definitions of the second SP of the pair specify the component's output performance to be achieved, considering input conditions as defined in the first SP. For example, a transmit converter component specification can be derived from SP1 and SP2. Receive converter component requirements are covered by SP3 and SP4. Wiring harness requirements can be derived from SP2 and SP3.

In addition to the definitions of the SPs for a point-to-point link, this document defines requirements covering the stability of the MOST network. Examples are requirements regarding jitter transfer through MOST devices, jitter accumulation through the MOST network, and power state transitions.

The specified parameters in this document are minimum values to ensure functionality of the MOST network in a wide range of environmental conditions.

7.3 Phase variation

7.3.1 General

Phase variation is caused by data stream timing noise and distortion.

7.3.2 Wander

Wander is made up of any phase variation from 0 Hz to 10 Hz. All active MOST components in the MOST network create wander. Wander is a function of the temperature drift and propagates from node to node. Typically, wander does not affect alignment jitter eye masks.

NOTE It is possible that the wander impacts the TimingMaster.

7.3.3 Jitter

Jitter is any phase variation of frequencies above 10 Hz. Every MOST component and the transmission medium create jitter in the MOST network. Jitter is correlated or uncorrelated. The dominant jitter

sources in the MOST network consist of PLL noise, link-induced DDJ, sensitivity-induced OEC noise, crosstalk, or phenomena such as power supply coupling. Data scrambling is used to eliminate DDJ correlation between nodes.

There are two jitter categories as shown in Figure 4:

— Alignment jitter: jitter that affects the reception of data by degrading the receiver eye diagram with horizontal closure (influences eye diagram measurement); it has impact only on a link as data recovery is performed by the MNC.

— Transferred jitter: jitter that is accumulated over all links (does not influence eye diagram measurement); the TimingMaster jitter tolerance shall be determined accordingly.

As the jitter on the measured signal increases, the eye closes more and more. A keep-out mask is specified to detect possible error traces. If the eye does not hit the mask then data recovery is ensured. Mask design depends on the required receiver margin and the characteristics of the channel.

Figure 4 shows the phase variation measurements.

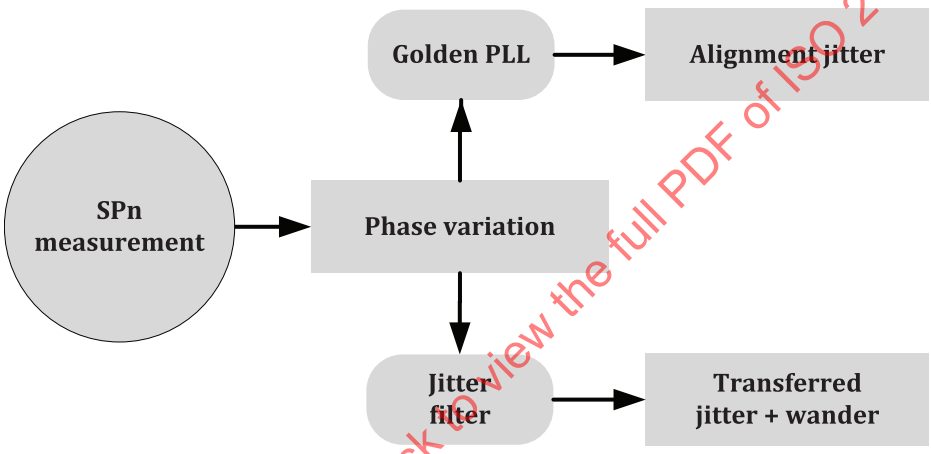


Figure 4 — Phase variation measurements

7.3.4 Clock recovery and reference clock

7.3.4.1 General

Phase variation can be measured directly on a data stream. To view alignment jitter and transferred jitter independently, special tools are required.

All MOST networks contain one device that implements the TimingMaster, which creates the reference clock. This clock is embedded within the data stream. All other MOST devices contain TimingSlaves that recover the clock from the data stream. Therefore, clock recovery is a basic functionality of an MNC. MOST components add a phase variation to the data stream. This degrades the reference clock.

Receiver jitter tolerance and jitter transfer are basic operation properties of any MNC. Alignment jitter is measured by means of an eye diagram formed with a Golden PLL. Transferred jitter is measured with a jitter filter.

Figure 5 illustrates clock recovery and data recovery in an MNC. Therefore, there is a need for a Golden PLL model and a jitter filter model. Together they reflect the required jitter behaviour of an MNC.

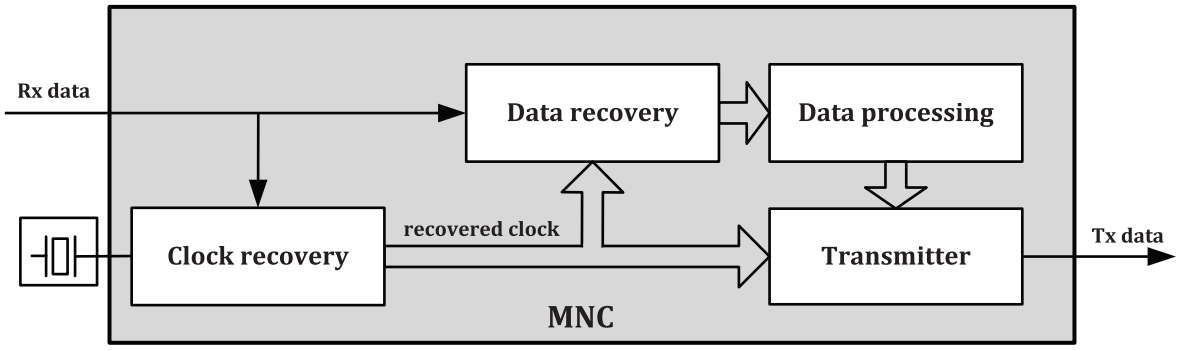


Figure 5 — Clock and data recovery example

7.3.4.2 Golden PLL

The Golden PLL is a simplified model which describes the behaviour of the MNC when jitter is applied to its input. A Golden PLL can be constructed out of hardware or software but shall obtain data from the SP and output a clock at the UI frequency for eye diagram formation.

7.3.4.3 Jitter filter

The jitter filter is a simplified model which describes the worst-case MNC jitter transfer function. A jitter filter can be constructed out of hardware or software but shall obtain data from the SP and output the RMS value of the transferred jitter at the SP.

7.3.5 Link quality

7.3.5.1 General

Link quality describes the minimum performance of MOST components along a single link.

7.3.5.2 Alignment jitter

Link quality eye diagrams are used to specify and measure link operation and MOST network level performance. A jitter budget is created top down starting from SP4. The difference between the SPs gives the tolerable contribution of alignment jitter for the respective MOST component or transmission medium. As an example, link quality eyes can be required at every point along the link to allow each MOST component's alignment jitter contribution to be specified. Figure 6 shows an example of the eye diagrams that correspond to the SPs in a link.

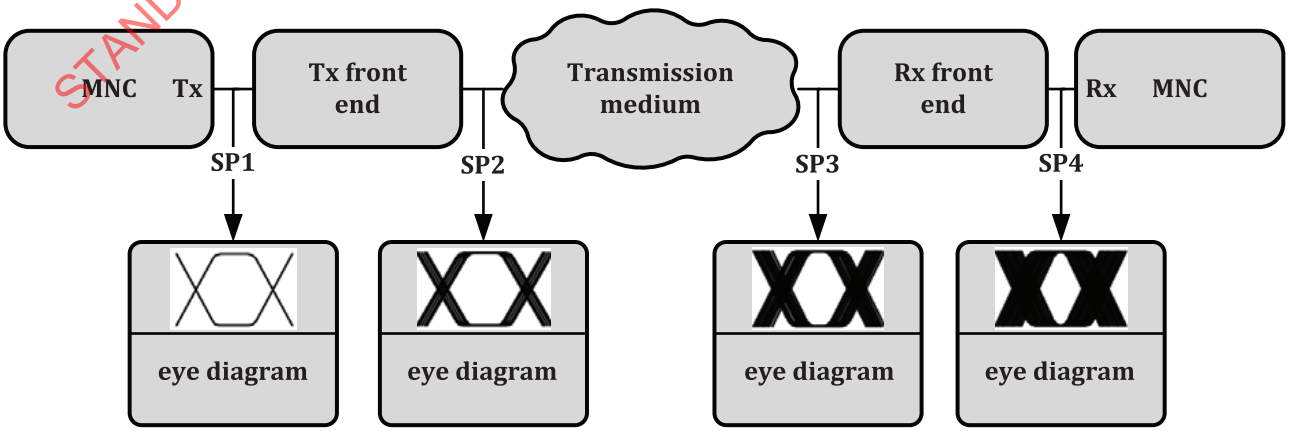


Figure 6 — Illustration of eye diagrams at SPs in a link

7.3.5.3 Transferred jitter

A portion of every jitter source in the MOST network has some spectral content below the jitter filter bandwidth. Jitter passed by the filter accumulates in the following nodes. Transferred jitter from all sources combines to form accumulated jitter. Accumulated jitter starts small with the first TimingSlave and gets larger towards the end of the ring. Therefore, the total jitter at the last SP4 point in the MOST network has two components, one being the total jitter generated in the final link, and the second being the accumulated jitter from all the links before. Each node shall limit its contribution to the accumulated jitter to prevent end-of-ring eye closure and receiver failure. The TimingMaster shall be able to tolerate the peak-to-peak swing of this accumulated jitter. Transferred jitter is critical to MOST network performance. Transferred jitter is measured by filtering the phase variation at any SPn with a jitter filter. The RMS (standard deviation) of the output of this jitter filter is the amount of jitter contributed to accumulated jitter. Transferred jitter specifications are placed at every SP as shown in Figure 7.

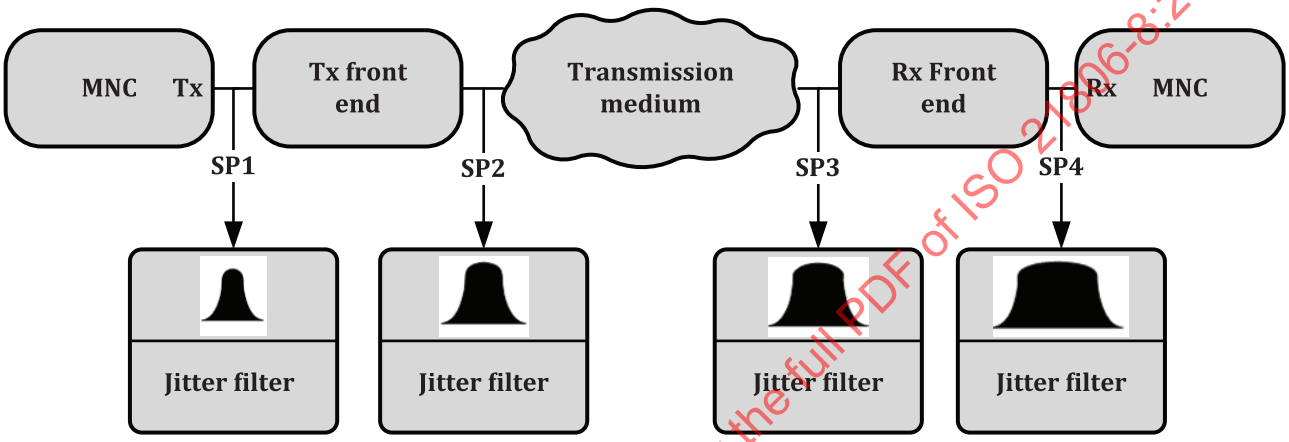


Figure 7 — Illustration of transferred jitter accumulation at various SPs in a link

7.3.6 MOST network quality

7.3.6.1 Receiver tolerance

Receiver tolerance describes the minimum alignment jitter tolerance of an MNC and the maximum tolerable alignment jitter that may occur at any place in the MOST network.

The minimum and maximum limits of the eye mask define the receiver tolerance. The closure of the eye mask originates from accumulated jitter in the MOST network. An MNC recovers all signals that fit into the SP4 receiver tolerance mask. A MOST device recovers all signals that satisfy the SP3 link quality requirements. Figure 8 shows the typical SPs in a ring where the SP4 receiver tolerance limits can be applied as a test of MOST network performance.

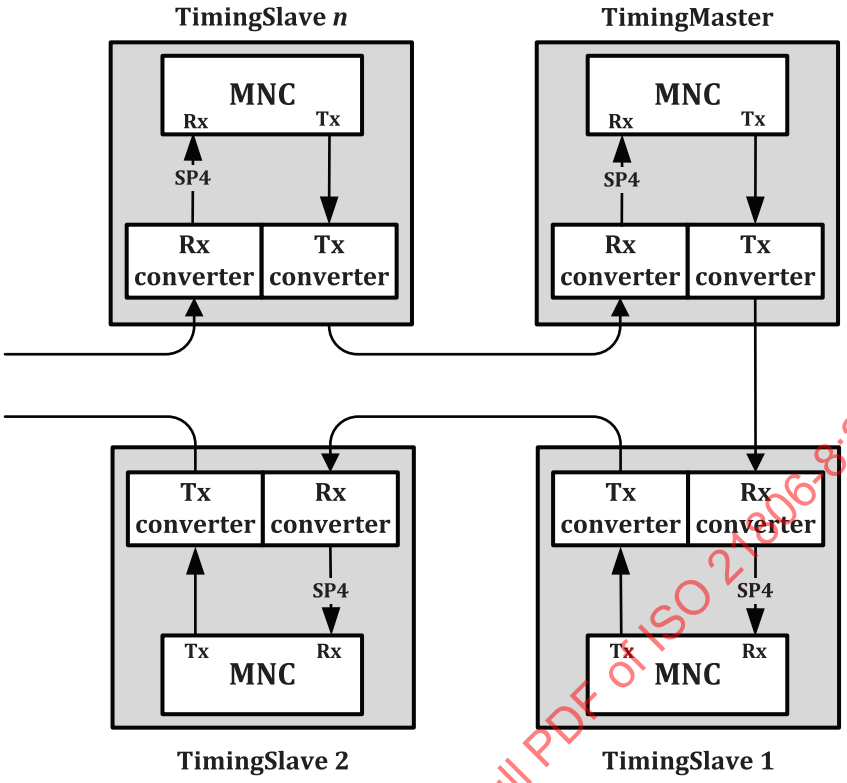


Figure 8 — Locations where receiver tolerance eye mask can be applied

7.3.6.2 TimingMaster delay tolerance

The MOST network stability is determined by the ability of the TimingMaster node to tolerate the accumulated delay present at the end of the ring. TimingMaster delay tolerance is the maximum amount of accumulated delay for an MNC that is configured as TimingMaster.

TimingMaster delay tolerance is tied to the delay, transferred jitter, transferred wander and maximum node count.

Formula (1) defines the minimum for the TimingMaster delay tolerance (t_{MDT}). The relevance of the different types of phase variation for the accumulated delay is shown in Table 8.

The requirements for the MOST network design are combined in the Formula (1) — TimingMaster delay tolerance t_{MDT}.

$$t_{MDT} \geq t_D(M) + \sum_{n=1}^{m-1} t_D(n) + \sum_{n=0}^{m-1} t_W(n) + t_{D\,Medium} + \alpha \times \sqrt{\sum_{n=0}^{m-1} \left[t_{TJ}(n)\right]^2} \quad (1)$$

where

t_{MDT} is the TimingMaster delay tolerance;

M is the position of the TimingMaster;

m is the number of nodes in the network;

n is the position of the node in the network;

$t_D(M)$ is the delay of the TimingMaster node caused by Rx and Tx converter;

$t_{D\ Medium}$ is the total delay caused by the medium;

α is a scaling factor that depends on the BER, see Table 8;

$t_D(n)$ is the delay of a TimingSlave node, see Table 8;

$t_W(n)$ is the wander (phase drift) of the node and link (peak-to-peak);

$t_{TJ}(n)$ is the transferred jitter of the node (RMS) (i.e. α = 12, derived from ±6 σ for BER = 10^{-9}).

Assumption

t_W is correlated from node to node;

t_{TJ} is uncorrelated from node to node.

Table 8 shows the purpose of the MOST network delay and jitter parameters that are combined in Formula (1).

Table 8 — MOST network delay and jitter parameters

Delay	Formula	Description
Delay of TimingMaster node	(2)	$t_D(M)$ is the delay caused by Rx and Tx converter of the TimingMaster node.
Delay of a TimingSlave node	(3)	A MOST network operates properly if the TimingMaster complies with this Formula.
Accumulation of delay of TimingSlave nodes	(4)	t_{DS} is the delay caused by the (m – 1) TimingSlave nodes. The delay per node is determined by the contribution of Rx converter, MNC and Tx converter.
Delay of the medium	$t_{D\ Medium}$	Total delay caused by the medium (e.g. depending on the length of the medium in use).
Accumulation of wander	(5)	t_{W_SUM} is the accumulated wander of all nodes. Due to the low-frequency characteristic of wander, either most or all of this phase variation is transferred by a PLL. Wander is generated by all active MOST components of the link and by the MNC chip. Wander is most commonly caused by variations in temperature. It shall be specified in the data sheet of each active MOST component.
Accumulation of transferred jitter	(6)	t_{TJ_SUM} is the accumulated transferred jitter of all nodes. Uncorrelated jitter sources add according to their variance. Scrambled data eliminates the correlation between DDJ on successive nodes. OEC noise and PLL noise sources are typically uncorrelated as well. This peak-to-peak number can be directly tied to a BER when the assumed jitter PDF is normal, e.g. α = 12 in case of ±6 sigma for BER = 10^{-9}.

$$t_D(M) = t_{D\,Rx}(M) + t_{D\,Tx}(M) \quad (2)$$

where

M is the position of the TimingMaster;

$t_D(M)$ is the delay of the node caused by Rx and Tx converter;

$t_{D\,Rx}(M)$ is the delay of the TimingMaster node caused by Rx converter;

$t_{D\,Tx}(M)$ is the delay of the TimingMaster node caused by Tx converter.

$$t_{D}(n)=t_{D\,Rx}(n)+t_{D\,MNC}(n)+t_{D\,Tx}(n) \tag{3}$$

where

n is the position of node in the network;

$t_D(n)$ is the delay of a TimingSlave node, see Table 8;

$t_{D\,Rx}(n)$ is the delay of the node n caused by Rx converter;

$t_{D\,MNC}(n)$ is the delay of the node n caused by MNC;

$t_{D\,Tx}(n)$ is the delay of the node n caused by Tx converter.

$$t_{DS}=\sum_{n=1}^{m-1} t_{D}(n) \tag{4}$$

where

t_{DS} is the accumulated delay of the TimingSlave nodes;

$t_D(n)$ is the delay of a TimingSlave node;

n is the position of node in the network;

m is the number of nodes in the network.

$$t_{W\_SUM}=\sum_{n=0}^{m-1} t_{W}(n) \tag{5}$$

where

t_{W_SUM} is the accumulated wander of all nodes;

$t_W(n)$ is the wander (phase drift) per node and link (peak-to-peak);

n is the position of node in the network;

m is the number of nodes in the network.

$$t_{TJ\_SUM}=\alpha\times\sqrt{\sum_{n=0}^{m-1}\left[t_{TJ}(n)\right]^{2}} \tag{6}$$

where

t_{TJ_SUM} is the accumulated transferred jitter of all nodes;

$t_{TJ}(n)$ is the transferred jitter per node (RMS) (i.e. α = 12, derived from ±6 sigma for BER = 10^{-9});

n is the position of node in the network;

m is the number of nodes in the network.

8 MOST150 oPHY requirements

8.1 General MOST network parameters

8.1.1 MOST network coding

8.1.1.1 General

The following subclauses describe a technique of encoding digital data called DCA coding, which shall be used in MOST150 oPHY.

8.1.1.2 Pulse characteristics

The MOST150 oPHY signal is scrambled and encoded using DCA coding. Data pulses range from 2 UI to 6 UI, yielding five different pulse widths, as shown in Figure 9.

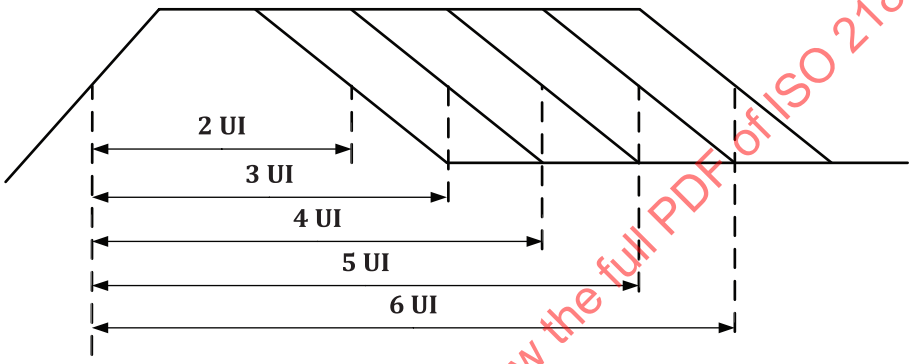


Figure 9 — Allowable pulse widths when using DCA coding

8.1.1.3 Unit interval definition

The unit interval (UI) width calculation is specified in Formula (7).

For MOST150 oPHY, there are 3 072 N_{BPF}. Using Formula (7) for a 48-kHz frame rate results in a UI of 3,391 ns. A 44,1-kHz frame rate has a UI of 3,691 ns.

$$t_{UI} = \frac{1}{\rho_{Fs} \times 2 \times N_{BPF}} \tag{7}$$

where

t_{UI} is the unit interval (UI);

ρ_{Fs} is the network frame rate;

N_{BPF} is the bits per frame.

8.1.1.4 DC balance

DCA coding ensures absence of DC. Short-term imbalances in offset occur during data transmission. These imbalances are tracked with a running total called the digital sum value (DSV). The DSV is calculated by incrementing the sum for every UI where the level is logic 1 and decrementing the sum for every UI where the level is logic 0. The calculation for DSV is illustrated in Figure 10.

Dynamic properties of DCA coding:

— The DSV is periodically driven to logic 0 at least once per frame.

— The range of DSV values in a valid DCA stream are {-5, -4, -3, -2, -1, 0, 1, 2, 3, 4, 5}.

— The shortest DCA period is 4 UI.

— The longest DCA period is 10 UI.

— The data stream shall have a period of 10 UI at least once per frame. These 10 UI periods can either be made of pulses that are 4 UI high/low with 6 UI low/high, 6 UI high/low with 4 UI low/high, or 5 UI high/low with 5 UI low/high.

Figure 10 shows the DSV calculation.

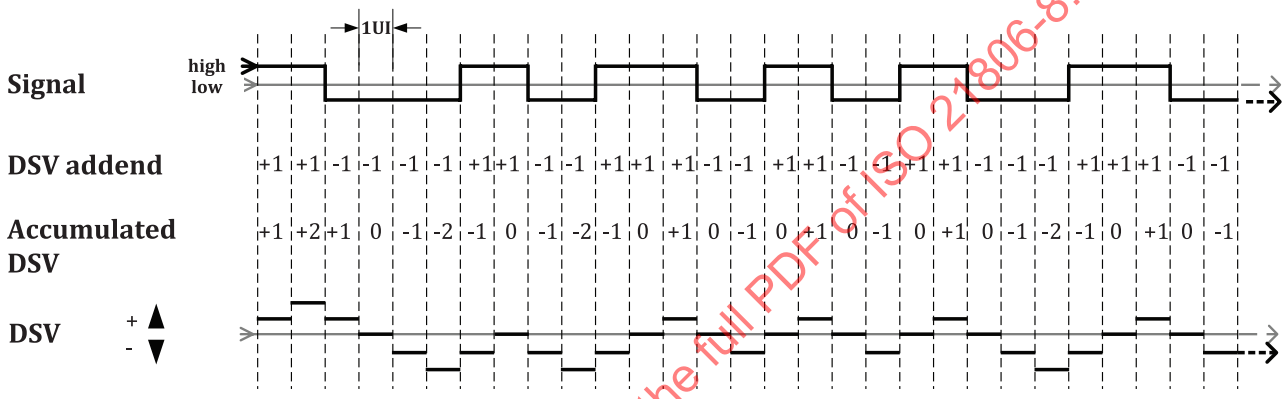


Figure 10 — DSV calculation

8.1.2 Specification Point details

Typically, an optical pigtail, a short piece of fibre or a light pipe, connects the FOR or FOX to the optical connector. The optical pigtail can cause some power loss between the converter and the optical connector. For more information about the optical connector, see Clause 14.

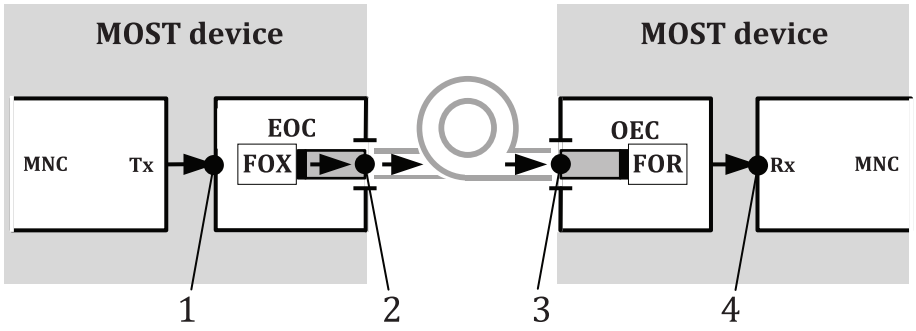
Table 9 specifies the SP locations and interfaces.

Table 9 — Specification point locations and interfaces

Specification Point	Location	Interface
SP1[a]	EOC electrical input pins including termination	LVDS
SP2[a]	End face of optical contact of optical connector	Radiated optical
SP3[a]	End face of optical contact of optical connector	Coupled optical
SP4[a]	OEC electrical output pins including termination	LVDS

[a] See Figure 6.

Figure 11 shows the location of specification points.



Key

1 SP1
2 SP2
3 SP3
4 SP4

Figure 11 — Location of specification points

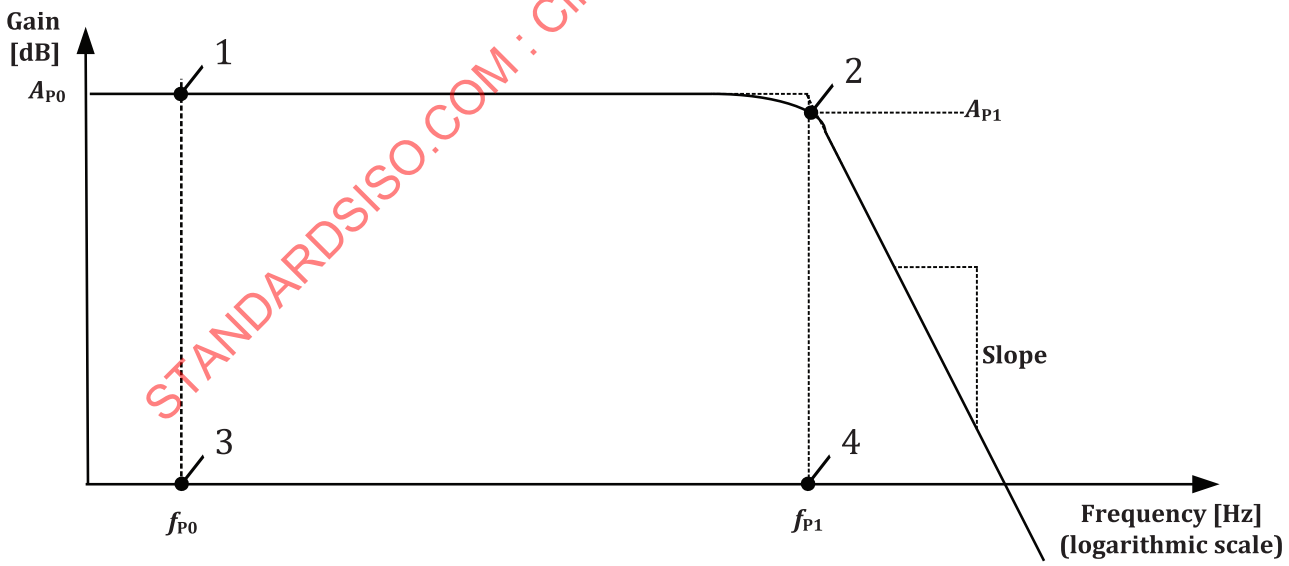
8.2 Models and measurement methods

8.2.1 Golden PLL

The Golden PLL determines the required worst-case jitter performance of an MNC and is used to form receiver eye diagrams. The positive edge of the signal shall trigger the Golden PLL. The transfer function is a low-pass filter with unity gain at 0 Hz.

NOTE For practicality of measurements, the transfer function is specified for 10 Hz and above.

Figure 12 shows the Golden PLL transfer function.



Key

1 amplitude point 0
2 amplitude point 1
3 frequency point 0
4 frequency point 1

Figure 12 — Golden PLL transfer function

Table 10 specifies the Golden PLL.

Table 10 — Golden PLL parameters

Parameter	Value	Unit
A_{P0}	0	dB
f_{P0}	10	Hz
A_{P1}	−3	dB
f_{P1}	125	kHz
Slope	−20	dB/dec

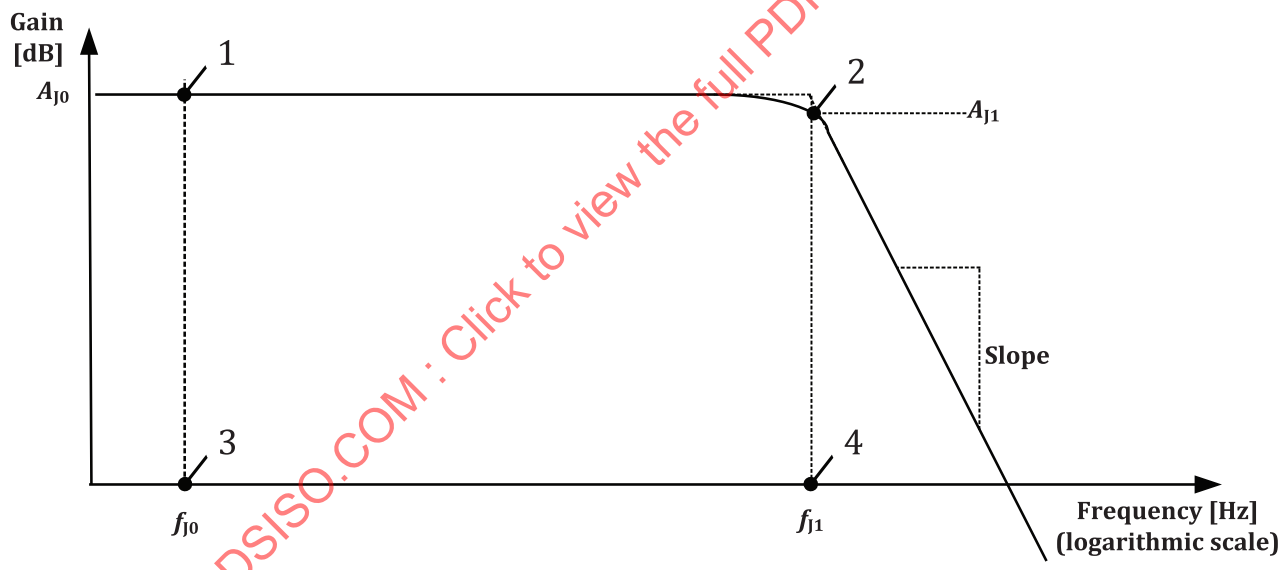
8.2.2 Jitter filter

The jitter filter determines the worst-case jitter transfer function of an MNC and is used to calculate transferred jitter along the link. The transfer function is a low-pass filter with unity gain at 0 Hz.

NOTE For practicality of measurements, the transfer function is specified for 10 Hz and above.

The jitter filter shall reference to the positive edge of the signal.

Figure 13 shows the jitter filter response.



Key

1 amplitude point 0
2 amplitude point 1
3 frequency point 0
4 frequency point 1

Figure 13 — Jitter filter response

Table 11 specifies the jitter filter specifications.

Table 11 — Jitter filter specifications

Parameter	Value	Unit
A_{J0}	0	dB
f_{J0}	10	Hz

Table 11 *(continued)*

Parameter	Value	Unit
A_{J1}	−3	dB
f_{J1}	200	kHz
Slope	−20	dB/dec

8.2.3 Retimed bypass mode and stress pattern

The retimed bypass mode is a test mode for physical layer testing. In retimed bypass mode, the MNC shall refresh and forward the received signal.

The MOST150 oPHY stress pattern shall be used for:

— optical signal level detection,

— optical overshoot and undershoot, and

— all eye diagrams.

Table 12 defines the reference of the MOST150 oPHY stress pattern.

Table 12 — Description of MOST150 oPHY stress pattern

Item	Item reference
Description code	MOST150 oPHY stress pattern
Filename	MOST150_Stress_Pattern-1v0.pat
Access location	ISO 21806-1:2020, Annex A
ZIP archive	MOST150_oPhy_Specification_1V1-0.zip

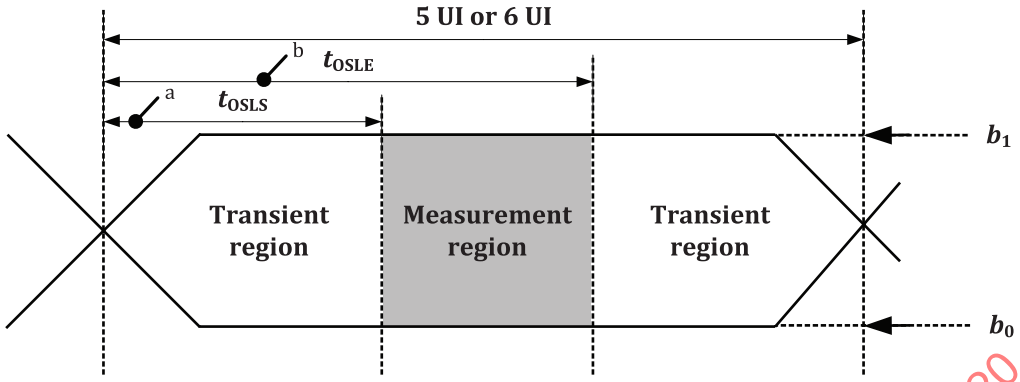
8.2.4 Optical signal level detection

Signal level detection of b_0 and b_1 shall calculate the extinction ratio and determine the placement of the SP2 and SP3 eye masks. The vertical amplitude of the SP2 and SP3 eye masks is scaled relative to the b_0 and b_1 levels.

8.2.5 Region of optical signal level detection

The b_1 level is determined during a 5 UI or 6 UI pulse with high optical signal level while the b_0 level is determined during a 5 UI or 6 UI pulse with low optical signal level. The transient regions are the areas of the pulse where the signal is not settled enough to yield a repeatable measurement for b_1 or b_0. The b_1 and b_0 values are the statistical mean of the high and low signal amplitude respectively during the interval defined in Figure 14 and Table 13.

Figure 14 shows the optical signal level test eye.



Key

a Time of optical signal level detection start.

b Time of optical signal level detection end.

Figure 14 — Optical signal level eye diagram

Table 13 specifies the optical signal level detection interval.

Table 13 — Optical signal level detection interval

Measurement region	Value	Unit
t_{OSLS}	2,5	UI
t_{OSLE}	4	UI

9 Link specifications

9.1 General

For jitter and pulse shape evaluation, this document specifies eye diagrams. A large eye opening indicates a signal with low jitter and distortion. The eye diagram is specified such that a valid signal does not overlap the eye mask. A signal that overlaps the eye mask does not meet the requirements. Signals with slow rise times, low amplitude, jitter, or pulse width variations are represented by closures in the eye diagram.

All MOST components along the link shall operate with a BER lower than 10^{-9}.

9.2 Specification Point 1 (SP1)

The signal at SP1 shall remain outside the keep-out areas of the eye mask. See 10.1, 11.4, and Clause 12 for operating conditions and interface specifications.

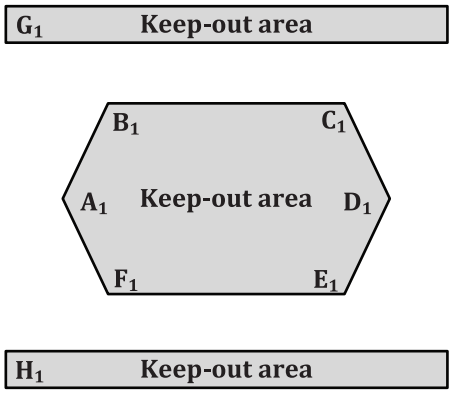
Table 14 specifies the link quality parameters of SP1.

Table 14 — Link quality parameters of SP1

Link quality parameters of SP1	Condition	Symbol	Minimum	Typical	Maximum	Unit
Transferred jitter (RMS)	Cd1[a]	J_{tr1}	---	---	50	ps
Eye mask (see Figure 15)	Cd2[b]	A_1 to H_1	---	---	---	---

[a] Use the jitter filter as specified in 8.2.2.

[b] Use the Golden PLL as specified in 8.2.1.



Key
A_1 to H_1 see Table 15

Figure 15 — Link quality parameters of SP1 — Eye mask

Table 15 specifies the link quality parameters of SP1 eye mask.

Table 15 — Link quality parameters of SP1 — Eye mask

Parameter (key)	Amplitude (mV)	Timing (UI)
A_1	0	0,075
B_1	+100	0,325
C_1	+100	0,675
D_1	0	0,925
E_1	−100	0,675
F_1	−100	0,325
G_1	+636	---
H_1	−636	---

9.3 Specification Point 2 (SP2)

9.3.1 Link quality parameters

The signal at SP2 shall meet the requirements in Table 16 and shall remain outside the keep-out area of the eye mask. Refer to 10.1, 11.4 and Clause 12 for operating conditions and interface standards.

Table 16 — Link quality parameters of SP2

Link quality parameters of SP2	Condition	Symbol	Minimum	Typical	Maximum	Unit
Centre wavelength	Cd1[a]	λ_{c2}	635	650	675	nm
Spectral width (RMS)	Cd2[b]	$\sigma_{\lambda 2}$	---	---	17	nm
Average optical output power	Cd3[c], Cd4[d], Cd5[e]	P_{opt2}	−8,5	---	−1,5	dBm
Extinction ratio	Cd6[f], Cd7[g]	r_{e2}	10	---	---	dB
Transition times (rise or fall)	Cd8[h]	t_{tr2}	---	---	0,5	UI
Transferred jitter (RMS)	Cd9[i]	J_{tr2}	---	---	112	ps
Eye mask (see Figure 16)	Cd6[j], Cd10[k]	A_2 to F_2 (see Table 17)	---	---	---	---

[a] The centre wavelength λ_{c2} is given in Formula (8).

[b] The spectral width $\sigma_{\lambda 2}$ is given in Formula (9).

[c] The laser Class 1 limits according with IEC 60825-2 shall be met. In failure cases, such as when no data transitions are present at the input of the transmitter, the output shall be disabled within the time t_{OFF2} (specified in Table 25).

[d] The power within a far field angle of 30° (NA = 0,5) and a diameter of 1 mm.

[e] The losses through the optical pigtail shall be kept below 1,5 dB, except integrated pigtail.

[f] The detection of b_0 and b_1 is specified in 8.2.4.

[g] The extinction ratio r_{e2} is given in Formula (10).

[h] The transition times are determined between the 20 % and 80 % thresholds.

[i] Use the jitter filter specified in 8.2.2.

[j] The detection of b_0 and b_1 is specified in 8.2.4.

[k] Use the Golden PLL specified in 8.2.1.

$$\lambda_{c2} = \frac{\sum_{i=\lambda_{start}}^{i=\lambda_{end}} P_i \times \lambda_i}{\sum_{i=\lambda_{start}}^{i=\lambda_{end}} P_i} \tag{8}$$

where

λ_{start} is 500 nm;

λ_{end} is 800 nm;

P_i is the optical power measured at the wavelength λ_i.

$$\sigma_{\lambda 2} = \sqrt{\frac{\sum_{i=\lambda_{start}}^{i=\lambda_{end}} P_i \times (\lambda_i - \lambda_{c2})^2}{\sum_{i=\lambda_{start}}^{i=\lambda_{end}} P_i}} \tag{9}$$

where

λ_{start} is 500 nm;

λ_{end} is 800 nm;

P_i is the optical power measured at the wavelength λ_i.

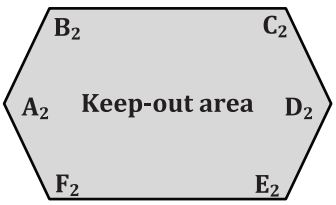
$$r_{e2} = 10 \times \log\left(\frac{b_1}{b_0}\right) \tag{10}$$

where

r_{e2} is the extinction ratio;

b_0 is the optical signal level when a logic 0 is transmitted;

b_1 is the optical signal level when a logic 1 is transmitted.



Key
A2 to F2 see Table 17

Figure 16 — Link quality parameters of SP2 — Eye mask

Table 17 specifies the link quality parameters of the SP2 eye mask.

Table 17 — Link quality parameters of SP2 — Eye mask

Parameter (Key)	Amplitude (mV)	Timing (UI)
A_2	$0{,}5 \times (b_1 + b_0)$	0,150
B_2	$0{,}8 \times (b_1 - b_0) + b_0$	0,400
C_2	$0{,}8 \times (b_1 - b_0) + b_0$	0,600
D_2	$0{,}5 \times (b_1 + b_0)$	0,850
E_2	$0{,}2 \times (b_1 - b_0) + b_0$	0,600
F_2	$0{,}2 \times (b_1 - b_0) + b_0$	0,400

9.3.2 Optical overshoot and undershoot

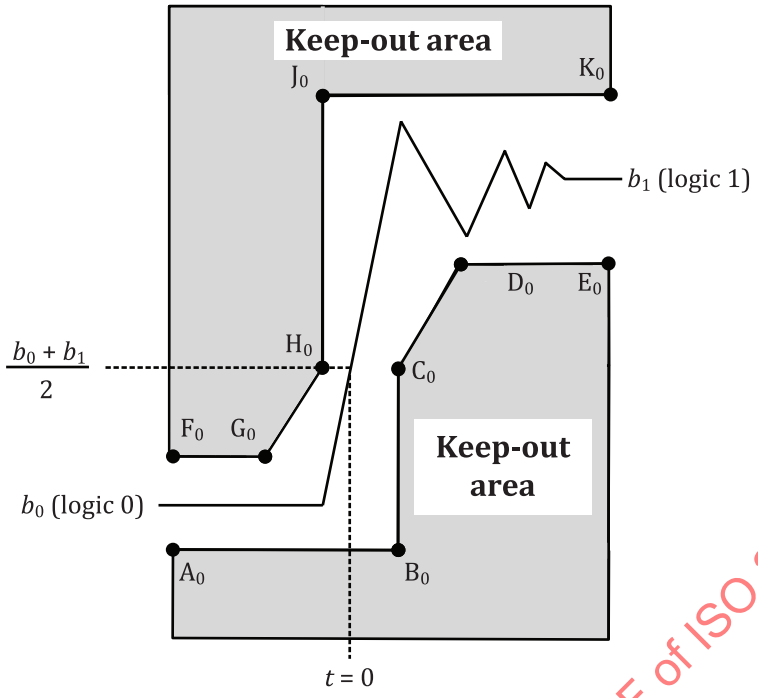
9.3.2.1 General

Measurement of the optical overshoot and undershoot ensures proper operation of the optical receiver. The optical pulse shape is tested with a parameterized mask. The mask parameters are based on b_0 and b_1. EOCs shall transmit an optical signal that complies with the specified overshoot and undershoot masks, when driven with an electrical signal as specified in 9.2.

9.3.2.2 Optical overshoot method

Mask amplitude parameters are normalized and are calculated based on the measured b_1 and b_0 levels. Time parameters are specified in units of UI and the origin is specified from the mid-point of the rising or falling edge of the signal, as illustrated in Figure 17 and Figure 18. The signal shall remain outside the keep-out areas of the masks.

Figure 17 shows the SP2 overshoot mask.



Key

A_0 to K_0see Table 18

Figure 17 — SP2 overshoot mask

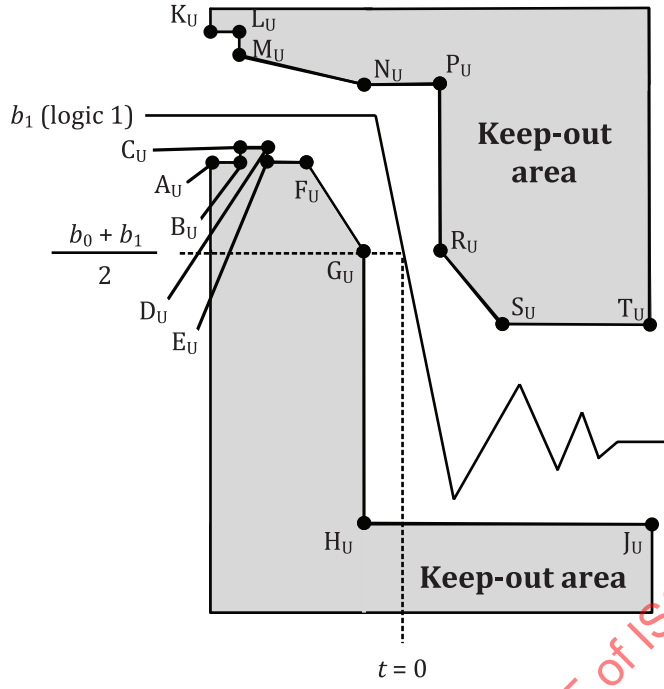
Table 18 specifies the SP2 overshoot mask parameter values.

Table 18 — SP2 overshoot mask parameter values

Mask parameter	Normalized amplitude	Time (UI)
A_0	−0,200	−0,630
B_0	−0,200	+0,100
C_0	+0,500	+0,100
D_0	+0,800	+0,350
E_0	+0,800	+1,370
F_0	+0,200	−0,630
G_0	+0,200	−0,350
H_0	+0,500	−0,100
J_0	+1,400	−0,100
K_0	+1,400	+1,370
NOTE All amplitude values are normalized to $b_0 = 0$ and $b_1 = 1$.		

9.3.2.3 Optical undershoot method

Figure 18 shows the SP2 undershoot mask.



Key

A_U to T_U see Table 19

Figure 18 — SP2 undershoot mask

Table 19 specifies the SP2 undershoot mask parameter values.

Table 19 — SP2 undershoot mask parameter values

Mask parameter	Normalized amplitude[a]	Time (UI)[b]
A_U	+0,800	−0,630 − x
B_U	+0,800	−0,530 − x
C_U	+0,850	−0,530 − x
D_U	+0,850	−0,430
E_U	+0,800	−0,430
F_U	+0,800	−0,350
G_U	+0,500	−0,100
H_U	−0,200	−0,100
J_U	−0,200	+1,370
K_U	+1,400	−0,630 − x
L_U	+1,400	−0,530 − x
M_U	+1,340	−0,530 − x

[a] All amplitude values are normalized to $b_0 = 0$ and $b_1 = 1$.

[b] The locations of A_U, B_U, C_U, K_U, L_U, and M_U on the time-axis depend on the nominal pulse width to be measured. This dependency is expressed by the parameter x, which is calculated by: x = nominal pulse width in UI − 2. (For 2 UI, $x = 0$; for 6 UI, $x = 4$).

Table 19 *(continued)*

Mask parameter	Normalized amplitude[a]	Time (UI)[b]
N_U	+1,150	−0,220 − *x*
P_U	+1,150	+0,100
R_U	+0,500	+0,100
S_U	+0,200	+0,350
T_U	+0,200	+1,370

[a] All amplitude values are normalized to $b_0 = 0$ and $b_1 = 1$.

[b] The locations of A_U, B_U, C_U, K_U, L_U, and M_U on the time-axis depend on the nominal pulse width to be measured. This dependency is expressed by the parameter x, which is calculated by: *x* = nominal pulse width in UI − 2. (For 2 UI, *x* = 0; for 6 UI, *x* = 4).

9.4 Specification Point 3 (SP3)

Applying the transfer function of the POF in Table 20, the stimuli for the receiver correspond to SP2 worst-case conditions. Refer to 10.1, 11.4 and Clause 12 for operating conditions and interface standards. OECs shall provide an electrical output signal as specified in 9.5. The signal at SP3 shall meet the requirements in Table 21.

Table 20 specifies the transfer function of optical fibre.

Table 20 — Transfer function of optical fibre

Transfer function of optical fibre	Condition	Mathematical representation of the POF link
3 dB bandwidth depending on L_{POF}	Cd1[a], Cd2[b], Cd3[c]	See Formula (11).
Standard deviation of Gaussian transfer function	Cd3[d]	See Formula (12).
POF transfer function	Cd4[e]	See Formula (13).

[a] For the calculation of SP3 stimulus minimum and maximum L_{POF} shall be considered.

[b] For the maximum length of POF see 11.3.

[c] L_{POF} is the length of the fibre in meter. The dimension of B_{3dB} is Hz.

[d] L_{POF} is the length of the fibre in meter. The dimension of B_{3dB} is Hz.

[e] The POF transfer function is valid for 1 mm polymer optical step index fibre with launch condition NA 0,5.

$$B_{3dB} = 1\,009 \times 10^6 \times L_{POF}^{-0,8747} \tag{11}$$

$$\sigma = 0,132 / B_{3dB} \tag{12}$$

$$|H|_{POF}(f) = \exp\left[-2 \times (\pi \sigma f)^2\right] \tag{13}$$

Table 21 specifies the link quality parameters of SP3.

Table 21 — Link quality parameters of SP3

Link quality parameters of SP3	Condition	Symbol	Minimum	Typical	Maximum	Unit
Centre wavelength	Cd1[a]	λ_{c3}	635	650	675	nm
Spectral width (RMS)	Cd2[b]	$\sigma_{\lambda 3}$	---	---	17	nm
Receivable average optical power range for data recovery	Cd3[c], Cd4[d], Cd5[e], Cd6[f], Cd7[g]	P_{opt3}	−22	---	−2	dBm
Receivable average optical power range for data recovery in LS version	Cd3[c], Cd4[d], Cd5[e], Cd6[f], Cd7[g]	P_{opt3LS}	−20	---	−2	dBm

[a] The centre wavelength λ_{c3} is given in Formula (14).

[b] The spectral width $\sigma_{\lambda 3}$ is given in Formula (15).

[c] The recommendations of IEC 60825-2 shall be taken into account when measuring SP3.

[d] The power within a far field angle of 30° (NA = 0,5) and a diameter of 1,0 mm.

[e] This assumes an attenuation of >0,5 dB between SP2 and SP3.

[f] The losses through the optical pigtail shall be kept below 1,5 dB, except integrated pigtail.

[g] This is the value when the incoming signal has passed the receiving contact end face.

NOTE The product type is provided with the label "MOST150 oPHY LS".

$$\lambda_{c3} = \frac{\sum_{i=\lambda_{start}}^{i=\lambda_{end}} P_i \times \lambda_i}{\sum_{i=\lambda_{start}}^{i=\lambda_{end}} P_i} \tag{14}$$

where

λ_{start} is 500 nm;

λ_{end} is 800 nm;

P_i is the optical power measured at the wavelength λ_i.

$$\sigma_{\lambda 3} = \sqrt{\frac{\sum_{i=\lambda_{start}}^{i=\lambda_{end}} P_i \times (\lambda_i - \lambda_{c3})^2}{\sum_{i=\lambda_{start}}^{i=\lambda_{end}} P_i}} \tag{15}$$

where

λ_{start} is 500 nm;

λ_{end} is 800 nm;

P_i is the optical power measured at the wavelength λ_i.

9.5 Specification Point 4 (SP4)

The signal at SP4 shall meet the requirements in Table 22 and shall remain outside the keep-out areas of the mask. Refer to 10.1, 11.4 and Clause 12 for operating conditions and interface standards.

Table 22 specifies the link quality parameters of SP4.

Table 22 — Link quality parameters of SP4

Link quality parameters of SP1	Condition	Symbol	Minimum	Typical	Maximum	Unit
Transferred jitter (RMS)	Cd1[a]	J_{tr4}	---	---	230	ps
Eye mask (see Figure 19)	Cd2[b], Cd3[c], Cd4[d]	A_4 ... H_4	---	---	---	---

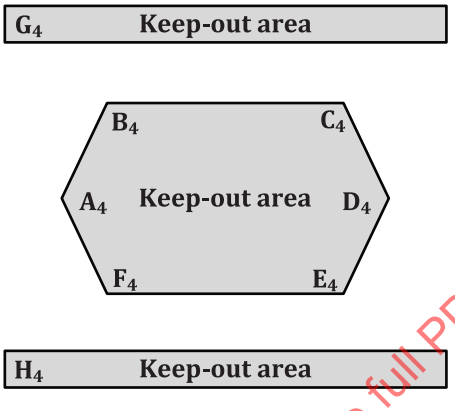
[a] Use the jitter-filter specified in 8.2.2.

[b] Use the Golden PLL specified in 8.2.1.

[c] The mask parameters include tolerances for overshoot and ringing.

[d] The steady-state differential voltage shall not be less than that specified in TIA/EIA-644-A.

Figure 19 shows the link quality parameters of SP4 eye mask.



Key

A_4 to H_4 see Table 23

Figure 19 — Link quality parameters of SP4 — Eye mask

Table 23 specifies the link quality parameters of SP4 eye mask.

Table 23 — Link quality parameters of SP4 — Eye mask

Parameter (Key)	Amplitude (mV)	Timing (UI)
A_4	0	0,275
B_4	+148	0,425
C_4	+148	0,575
D_4	0	0,725
E_4	−148	0,575
F_4	−148	0,425
G_4	+636	---
H_4	−636	---

10 Power-on and power-off

10.1 Frequency reference and power supply

The MOST device shall provide the following:

— Frequency reference: the frequency reference is typically a crystal-controlled oscillator or derivative. The requested accuracy is specified in 12.2.

— Power supply:

  — V_{CCTX}: MNC and EOC supply with a nominal operating range as specified in Table 25. The power supply shall be capable of being switched off.

  — V_{CCRX}: permanent power supply for the OEC with a nominal operating range as specified in Table 26. It is typically provided by a supply independent from V_{CCTX}.

  — Power supply monitoring circuitry: the MOST device shall provide power supply monitoring circuitry for supervising V_{CCTX} which is specified in 10.2. The MOST device shall connect the active-low reset signal /RST provided by the power supply monitoring circuitry to the /RST inputs of the EOC and the MNC.

10.2 Power supply monitoring circuitry

The power supply monitoring circuitry shall:

— provide an active-low reset signal/RST that is a valid LVTTL (JESD8C) signal over the power supply range V_{VALID} specified in Table 24;

— set the /RST signal to logic 1 when the power supply voltage ramps above the V_T threshold. Switching from logic 0 to logic 1 shall be delayed by a minimum time of t_{D+} to allow the circuitry in the EOC to stabilize, the LVDS pins of the MNC to be driven, and the local frequency reference to stabilize. Although a maximum time for t_{D+} is not specified, an implicit maximum value exists due to the required startup time (light-in to light-out);

— set the /RST signal to logic 0 when the voltage drops below the threshold V_T. Switching from logic 1 to logic 0 shall occur within a time of t_{D-}.

Table 24 specifies the /RST signal parameters.

Table 24 — /RST signal generation

/RST signal	Condition	Symbol	Minimum	Typical	Maximum	Unit
Supply range for valid logic levels	---	V_{VALID}	1	---	3,465	V
Logic switching threshold	---	V_T	2,97	---	---	V
Logic 0 to logic 1 time delay	---	t_{D+}	1	---	---	ms
Logic 1 to logic 0 time delay	---	t_{D-}	0	---	100	µs

10.3 Optical and electrical signal power state

10.3.1 General

Optical wake-up and shutdown methods of the MOST network require certain functionality to be built into the EOC and OEC MOST components.

10.3.2 EOC requirements

The EOC functional requirements are listed below:

a) The EOC shall have an LVTTL (JESD8C) reset bar (/RST) input pin.

b) The EOC shall be capable of performing transition detection at its input. Transition detection is the ability to monitor the input frequency of the signal at SP1 and make a logical decision as to whether the frequency meets the specifications of F_{OFF1} or F_{ON1}.

c) The off-state for the EOC is specified as follows:

  — The EOC shall not output optical power above P_{OFF2}.

— The EOC shall perform transition detection at SP1 in order to check for a valid wake-up condition, defined as the input signal frequency being within F_{ON1}.

d) The on-state for the EOC is specified as follows:

— The EOC shall produce an optical output that is compliant with all the SP2 parameters defined in Table 16 when being driven by valid SP1 data.

— The EOC shall perform transition detection at SP1 in order to check for a valid shutdown condition, defined as the input signal frequency being within F_{OFF1}.

e) The EOC shall not generate any optical signals exceeding P_{OFF2} when being supplied with an operating voltage within $V_{CCTXOFF}$ regardless of the state of the SP1 and /RST inputs.

f) The EOC shall not generate any optical signals exceeding P_{OFF2} when the /RST input is logic 0.

g) When being supplied with an operating voltage within V_{CCTXGR}, the internal circuitry of the EOC shall settle into stable operation with the ability to perform transition detection within a time defined by the minimum value of the parameter t_{D+} and activate SP2 output.

h) When being supplied with an operating voltage within V_{CCTXOR}, the EOC shall settle into operation defined as the on-state, within a time t_{ON2} when

— the /RST input pin is set to logic 1, and

— the frequency of the SP1 signal is within F_{ON1} (transition detection).

i) When being supplied with an operating voltage within V_{CCTXGR}, the EOC shall be capable of performing transition detection and shall enter the off-state, within a time t_{OFF2} when

— the /RST input pin is driven logic 0, or

— the frequency of the SP1 signal is within F_{OFF1} (transition detection).

j) In the frequency range F_{ON1}, the EOC shall be in the on-state. In the frequency range F_{OFF1}, the EOC shall be in the off-state. The transition is performed between F_{OFF1} maximum and F_{ON1} minimum.

The EOC requirements are summarized in Table 25. Refer to Figure 20 for more details.

Table 25 — EOC power state requirements

EOC power state requirements	Condition	Symbol	Minimum	Typical	Maximum	Unit
EOC operating voltage range	---	V_{CCTX}	3,135	3,300	3,465	V
EOC glitch-safe voltage range	---	V_{CCTXGR}	2,970	---	3,465	V
EOC off-state voltage range	---	$V_{CCTXOFF}$	0	---	1	V
EOC on-state frequency range at SP1	Cd1[a]	F_{ON1}	12	---	73,743	MHz
EOC off-state frequency range at SP1	---	F_{OFF1}	0	---	10	kHz
EOC power-on delay	Cd3[b]	t_{ON2}	---	---	100	µs
EOC power-off delay	---	t_{OFF2}	---	---	2	µs
Average optical output power for the off-state	Cd2[c]	P_{OFF2}	---	---	−50	dBm

[a] The EOC can still be in the on-state above this frequency.

[b] See 10.3.2 h).

[c] This is the power within a far field angle of 30° (NA = 0,5) and a diameter of 1 mm.

Figure 20 shows the EOC timing diagram.

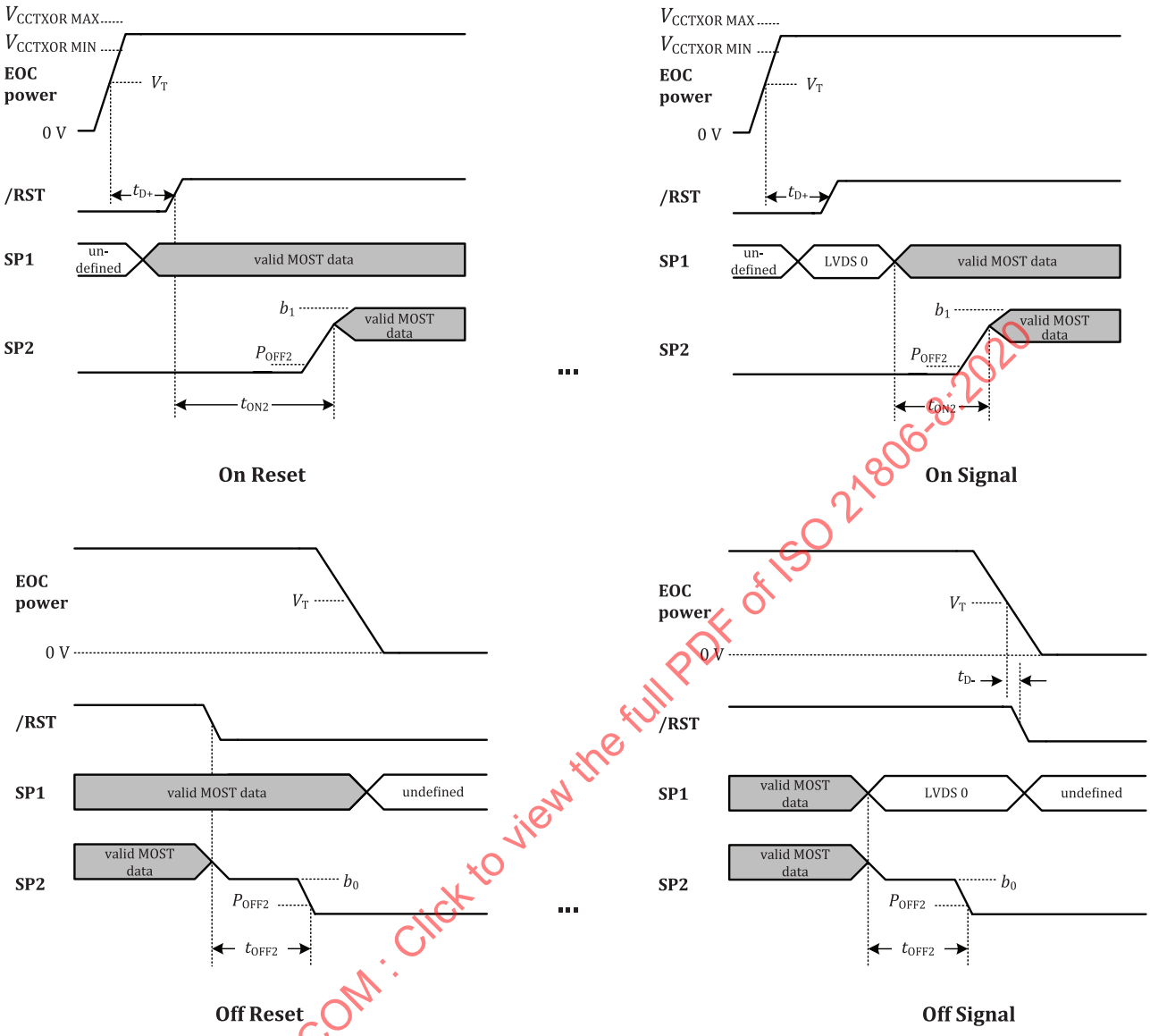


Figure 20 — EOC timing diagram

10.3.3 EOC power-on and power-off sequence

10.3.3.1 General

A typical power-on sequence and a typical power-off sequence for the EOC are described below and are referenced to Figure 20. Figure 20 shows an EOC timing diagram. Valid MOST data is specified as follows:

— For SP1, valid MOST data shall be DCA encoded data that meets the link quality parameters defined in Table 14 and the bit rate requirements defined in Table 31.

— For SP2, valid MOST data shall be DCA encoded data that meets the link quality parameters defined in Table 16, Table 18, Table 19 and the bit rate requirements defined in Table 31.

10.3.3.2 Power-on sequence example scenarios

The power-on sequence starts with the power supply voltage to the MNC and EOC ramping up. During the time at which the power supply voltage is not within the EOC's normal operating range, the /RST pin is pulled to logic 0 by the power supply monitoring circuitry to prevent optical glitches from being

generated at SP2. After the supply voltage reaches its normal operating level, the circuitry inside the MNC and EOC might not be stabilized. The power supply monitoring circuitry provides a time delay from when the supply voltage has reached its normal operating value until /RST transitions to logic 1 so that the local frequency reference, MNC circuitry, and EOC circuitry have time to stabilize. Some time after the power supply reaches its typical value, the local frequency reference stabilizes and valid LVDS logic levels are generated by the MNC at SP1. Once the proper frequency is detected at SP1, and /RST is logic 1, the EOC can then drive valid data on SP2.

10.3.3.3 Power-off sequence example scenarios

The normal power-off sequence is initiated by SP1 traffic being driven to logic 0 by the MNC. The EOC detects this event using its internal transition detection circuit and disables the output by driving SP2 to a power level below P_{OFF2} within the required time. The power supply to the EOC is shut down some time later. During the ramp down of the power supply, the /RST pin transitions to logic 0 before the EOC's power supply drops below the glitch-safe voltage range, preventing any glitches on the output at SP2. The /RST signal is valid down to the minimum of V_{VALID}. Below the minimum of V_{VALID}, the EOC is responsible for preventing any light output at SP2 regardless of the state of /RST.

10.3.4 OEC requirements

10.3.4.1 OEC functional requirements

The listed requirements are applicable for the OEC when being powered by an operating voltage in the range defined by V_{CCRXOR} in Table 26.

a) The OEC shall provide an output pin (STATUS) in accordance with LVTTL (LVTTL as shown in JEDEC No. JESD8C.01).

b) An OEC in the off-state

   — shall keep its STATUS logic 1, the SP4 bus disabled, and consume no more than the sleep current, $I_{CCSLEEP}$, and

   — shall monitor the optical input power and frequency at SP3.

   Current consumption may exceed $I_{CCSLEEP}$ if the OEC is being exposed to light above the range P_{OFF3} with a frequency below the range F_{ON3}.

c) An OEC in the on-state

   — shall keep its STATUS logic 0,

   — shall provide valid output data that meets the SP4 requirements in Table 22 when receiving valid data at SP3, and

   — shall monitor the optical input power and frequency at SP3.

d) An OEC shall transition from the off-state to the on-state upon detecting valid wake-up conditions, defined as an SP3 signal with optical power greater than P_{ON3} and a frequency within F_{ON3} as specified in Table 26. The wake-up procedure has the following requirements:

   — After valid wake-up conditions are detected at SP3, the OEC shall transition to STATUS logic 0 within time t_{STATF}.

   — After STATUS transitions to logic 0, the OEC shall enable the SP4 LVDS bus and produce a valid LVDS signal within time t_{LVDSV4}.

   — After valid wake-up conditions are detected at SP3, the OEC shall enter the on-state within time t_{ON4}.

e) An OEC in the on-state shall constantly monitor the input power level and signal frequency and shall transition to the off-state upon detecting valid shutdown conditions. When the signal at SP3 has optical power less than P_{OFF3} or a frequency within F_{OFF3} as specified the OEC shall be in off-state. The transition procedure to the off-state has the following requirements:

   — After valid shutdown conditions are detected at SP3, the OEC shall force the signal at SP4 to LVDS 0 and set STATUS logic 1 within time t_{STATR}. The OEC shall maintain a valid LVDS signal during the detection phase.

   — After STATUS transitions to logic 1, the OEC shall maintain its LVDS output at logic 0 for a hold time of t_{LVDSH4}.

   — After valid shutdown conditions are detected at SP3, the OEC shall enter the off-state within time t_{OFF4}.

f) In the frequency range F_{ON3}, the OEC shall be in the on-state. In the frequency range F_{OFF3}, the OEC shall be in the off-state. The transition is performed between F_{OFF1} maximum and F_{ON3} minimum.

In the power range P_{ON3}, the OEC shall be in the on-state. In the power range P_{OFF3}, the OEC shall be in the off-state. The transition is performed between P_{OFF3} maximum and P_{ON3} minimum.

10.3.4.2 OEC power state requirements

Table 26 specifies the OEC power state parameters. Table 25 specifies additional OEC power state parameters.

Table 26 — OEC power state requirements

Power state	Parameter	Condition	Symbol	Minimum	Typical	Maximum	Unit
Power-on	Average optical input power range for on-state operation	Cd1[a]	P_{ON3}	−22	---	−2	dBm
	Frequency range of input at SP3 for on-state operation	Cd2[b]	F_{ON3}	12	---	73,743	MHz
	OEC power-on delay	Cd3[c]	t_{ON4}	---	---	10	ms
	Delay to STATUS falling	Cd5[d]	t_{STATF}	200	---	1 000	µs
	STATUS falling to LVDS valid	---	t_{LVDSV4}	---	---	100	µs
	OEC operating voltage range	---	V_{CCRX}	3,135	3,300	3,465	V

a This is the power within a far field angle of 30° (NA = 0,5) and a diameter of 1,0 mm.

b The OEC can still be in the on-state above this frequency.

c t_{ON4} is the sum of t_{STATF}, t_{LVDSV4} and an additional time required for SP4 to be valid MOST traffic.

d The time from valid wake-up condition to STATUS logic 0, see 10.3.4.1 d).

e t_{OFF4} is the sum of t_{STATR} and t_{LVDSH4}.

f The time from detection of valid shutdown conditions at SP3 to STATUS logic 1, see 10.3.4.1 e).

g At −40 °C to 70 °C.

h At 70 °C to 95 °C.

Table 26 *(continued)*

Power state	Parameter	Condition	Symbol	Minimum	Typical	Maximum	Unit
Power-off	Average optical input power range for off-state operation	Cd1[a]	P_{OFF3}	-∞	---	–35	dBm
	Frequency range of input at SP3 for off-state operation	---	F_{OFF3}	0	---	10	kHz
	OEC power-off delay	Cd4[e]	t_{OFF4}	---	---	1	ms
	OEC LVDS hold time	---	t_{LVDSH4}	1	---	---	µs
	Delay to STATUS rising	Cd6[f]	t_{STATR}	---	---	2	µs
	Current consumption in the off-state	Cd7[g]	$I_{CCSLEEP}$	---	---	30	µA
	Current consumption in the off-state	Cd8[h]	$I_{CCSLEEP}$	---	---	45	µA

[a] This is the power within a far field angle of 30° (NA = 0,5) and a diameter of 1,0 mm.

[b] The OEC can still be in the on-state above this frequency.

[c] t_{ON4} is the sum of t_{STATF}, t_{LVDSV4} and an additional time required for SP4 to be valid MOST traffic.

[d] The time from valid wake-up condition to STATUS logic 0, see 10.3.4.1 d).

[e] t_{OFF4} is the sum of t_{STATR} and t_{LVDSH4}.

[f] The time from detection of valid shutdown conditions at SP3 to STATUS logic 1, see 10.3.4.1 e).

[g] At –40 °C to 70 °C.

[h] At 70 °C to 95 °C.

Figure 21 shows the OEC timing diagram.

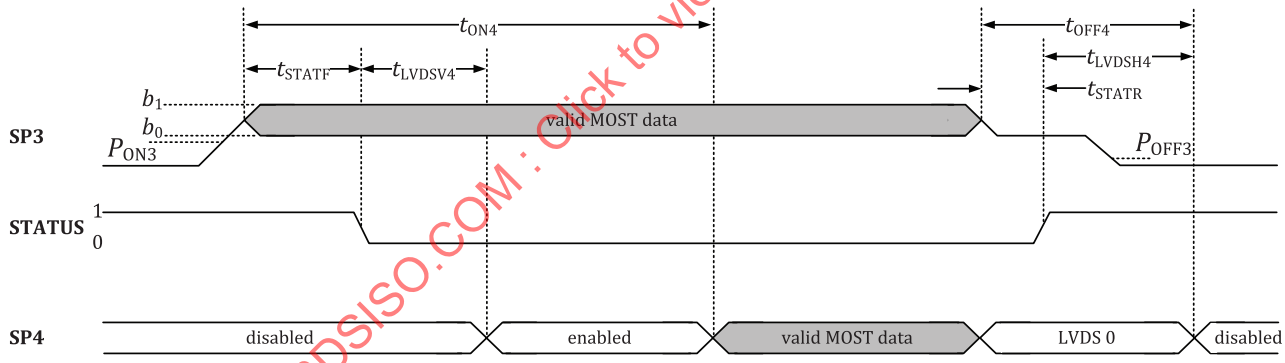


Figure 21 — OEC timing diagram

10.3.5 OEC power-on and power-off sequence

10.3.5.1 General

The typical power-on sequence and a typical power-off sequence for the OEC are described below. Figure 21 shows an OEC timing diagram. Valid MOST data is specified as follows:

— For SP3, valid MOST data shall be DCA-encoded data according to the link quality parameters specified in Table 21 and the bit rate parameters specified in Table 31.

— For SP4, valid MOST data shall be DCA-encoded data according to the link quality parameters specified in Table 22 and the bit rate requirements specified in Table 31.

10.3.5.2 Power-on sequence example scenario

An OEC that is in the off-state monitors the input signal at SP3. The OEC verifies that the optical power and signal frequency meet specifications before exiting the off-state. If valid wake-up conditions are present, the OEC sets STATUS logic 0, enables the SP4 LVDS bus. After a settling time, valid LVDS logic levels are present although valid MOST data may not be on the bus yet. After a short period, the OEC is fully on and valid MOST data is on the SP4 bus.

10.3.5.3 Power-off sequence example scenario

An OEC that is in the on-state monitors the input power level and signal frequency at SP3. If either the power level or frequency does not meet specifications, the OEC begins transitioning to the off-state by setting the SP4 output to LVDS 0 and setting STATUS logic 1. The SP4 bus is then maintained at LVDS 0 for a hold time while STATUS is logic 1. After this hold time, the OEC disables the SP4 bus and enters the off-state.

11 MOST network requirements

11.1 SP4 receiver tolerance

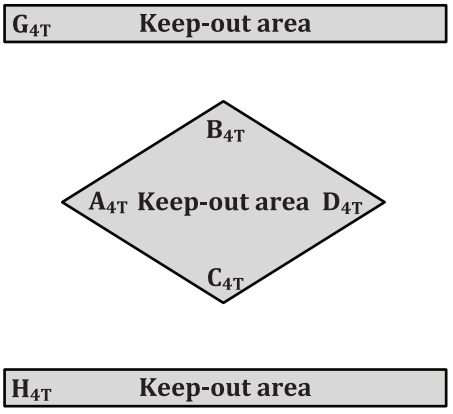
All MOST components along the link shall operate with a bit error rate (BER) lower than 10^{-9}. See 10.1, 11.4, and Clause 12 for operating conditions and interface standards.

Table 27 specifies the receiver tolerance parameters of SP4.

Table 27 — Receiver tolerance parameters of SP4

Receiver tolerance SP4	Condition	Symbol	Minimum	Typical	Maximum	Unit
Eye mask (see Figure 22)	Cd1[a], Cd2[b], Cd3[c]	A_{4T} ... H_{4T}	---	---	---	---
[a] Use the Golden PLL as specified in 8.2.1.						
[b] The difference between the SP4-eye mask and the SP4 receiver tolerance eye mask in the horizontal timing direction is due to accumulated jitter along the link.						
[c] The additional vertical closure on the mask is caused by the large amount of jitter present on the signal. The signal shall still comply with the LVDS specification regarding the minimum signal amplitude.						

Figure 22 shows the receiver tolerance parameters of SP4 eye mask.



Key

A_{4T} to H_{4T} see Table 28

Figure 22 — Receiver tolerance parameters of SP4 — Eye mask

Table 28 specifies the receiver tolerance parameters of SP4 eye mask.

Table 28 — Receiver tolerance parameters of SP4 — Eye mask

Parameter (Key)	Amplitude (mV)	Timing (UI)
A_{4T}	0	0,300
B_{4T}	80	0,500
C_{4T}	−80	0,500
D_{4T}	0	0,700
G_{4T}	636	---
H_{4T}	−636	---

11.2 TimingMaster delay tolerance

The TimingMaster delay is the sum of all static phase (delay) and phase variation measured between the Rx input relative to the Tx output of the TimingMaster. The TimingMaster delay tolerance and the node count shall not exceed the maximum values specified in Table 29.

Table 29 — TimingMaster delay tolerance requirements

/RST signal	Condition	Symbol	Minimum	Typical	Maximum	Unit
Node count	---	N	---	---	20	---
TimingMaster delay tolerance	---	t_{MDT}	---	---	$\frac{0,5}{\rho_{Fs}}$	µs

11.3 Optical fibre link length requirement

The maximum node-to-node link length shall be 15 m.

11.4 Environmental requirements and considerations

For the EOC and OEC, the operating temperature range shall be T_A = −40 °C to +95 °C.

The temperature at SP2 and SP3 of the ECU shall not exceed T_A = +85 °C, based on the maximum allowed temperature of the POF harness.

NOTE Ambient conditions (automotive worst-case conditions) for the ECU like humidity, vibration and shock, resistance against chemical agents, EMC/EMI, and ECU lifetime are not in the scope of this document. FOT and pigtail comply with the appropriate automotive application recommendation[5][6]. MNCs are characterised and qualified according to the AEC-Q100 Rev–H. MOST components and MOST devices are developed to an EMC-optimized design.

12 Electrical interfaces

12.1 LVDS

Rx data and Tx data electrical interfaces of MOST components shall be LVDS compliant as specified in TIA/EIA-644-A. One exception is listed in Table 30. All PCB-level Rx data and Tx data electrical interfaces shall be designed such that MOST components compliant with LVDS operate correctly. This requirement applies to MOST components on PCB-level. It does not apply to the wiring harness. All electrical signals shall maintain the correct polarity from OEC to MNC and from MNC to EOC. Table 30 specifies the exception regarding LVDS.