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**Cards and security devices for
personal identification—Test
methods—**

**Part 6:
Contactless proximity objects**

**AMENDMENT 1: Dynamic power level
management**

*Cartes et dispositifs de sécurité pour l'identification personnelle —
Méthodes d'essai —*

Partie 6: Objets sans contact de proximité

AMENDEMENT 1: Gestion dynamique de niveau de puissance

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This document was prepared by Joint Technical Committee ISO/IEC JTC 1, *Information technology*, Subcommittee SC 17, *Cards and security devices for personal identification*.

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Cards and security devices for personal identification — Test methods —

Part 6: Contactless proximity objects

AMENDMENT 1: Dynamic power level management

Page 3, 3.2

Add the following symbols:

" H_0 PCD field strength during power level management test procedures"

Page 7, 4.7, Table 3

Add the following two rows after the row for "Optional PICC classes":

"

| Parameter | Description | Unit |
|--|---|------|
| Support of PLI _{ATQ} handling | Ability to change power level (and therefore field strength) after receiving PLI _{ATQ} from a PICC | |
| Support of PLI _{CID} handling | Ability to change power level (and therefore field strength) after receiving PLI _{CID} from a PICC | |

"

Page 8, 4.8, Table 6

Replace Table 6 with the following table:

"

Table 6 — PICC manufacturer information

| Parameter | Description | Unit |
|--|--|------|
| Location, center and size of the antenna | Drawing with dimensions of the PICC outside shape and the position of the external rectangle/circle of the claimed PICC class. | |
| PICC class (optional) ^a | Claimed PICC class | |
| Resonance frequency range (optional) | Minimum and maximum resonance frequency | MHz |
| Communication signal interface | Supported communication signal interface(s): — Type A — Type B — Type A and Type B | |

^a If not provided, test methods for Class 1 shall be used

Table 6 (continued)

| Parameter | Description | Unit |
|---|---|-------|
| Temperature range | Minimum and maximum temperature values | °C |
| Supported PLI _{ATQ} values | List of supported optional PLI _{ATQ} values in Answer to Request | |
| Supported PLI _{CID} values | List of supported optional PLI _{CID} values in CID field | |
| PCD to PICC supported bit rates | List of supported optional PCD to PICC bit rates | |
| PICC to PCD supported bit rates | List of supported optional PICC to PCD bit rates | |
| Same bit rate for both directions | Indication if only same bit rate from PCD to PICC and from PICC to PCD is supported | |
| Random or fixed UID (Type A) or PUPI (Type B) | Indication whether the UID (Type A) or PUPI (Type B) is random or fixed | |
| Maximum frame size supported | Maximum frame size in reception | bytes |
| PCD to PICC frame with error correction supported | Frame with error correction from PCD to PICC | |
| PICC to PCD frame with error correction supported | Frame with error correction from PICC to PCD | |
| TEST_COMMAND_SEQUENCE1 | See 0.2.1 | |
| TEST_COMMAND1 | See 0.2.1 | |
| TEST_COMMAND2 | See 0.2.1 | |
| TEST_COMMAND3 | See 0.2.1 | |
| TEST_COMMAND4 | See 0.2.1 | |

^a If not provided, test methods for Class 1 shall be used

"

Page 38, 7.1.9

Add the following subclause after 7.1.8.3:

"

7.1.9 Procedures for PCD supporting optional PLI_{ATQ} or PLI_{CID} handling

7.1.9.1 Scope

These tests apply only to PCDs which support PLI_{ATQ} or PLI_{CID} handling.

If the PCD supports optional PLI_{ATQ} or PLI_{CID} handling, the additional procedures specified in 7.1.9.2, 7.1.9.3, 7.1.9.4 and H.5 shall be used to verify that, for every power level used by the PCD:

- the PCD complies with the field strength requirements specified in ISO/IEC 14443-2:2020/Amd 1, ISO/IEC 14443-3:2018/Amd 1 and ISO/IEC 14443-4:2018/Amd 1;
- the PCD complies with modulation index and waveform requirements specified in ISO/IEC 14443-2;
- the PCD complies with load modulation reception requirements specified in ISO/IEC 14443-2;
- the PCD complies with EMD immunity requirements specified in ISO/IEC 14443-2.

7.1.9.2 Modulation index and waveform

The steps c) to g) of the procedure specified in 7.1.4.2 shall be repeated for every power level between minimum and maximum power level obtained by PLI_{ATQ} or PLI_{CID}.

For each power level, the test report shall be as specified in 7.1.4.3.

7.1.9.3 Load modulation reception

The procedures specified in 7.1.6.5 and 7.1.6.6 shall be repeated for every power level between minimum and maximum power level obtained by PLI_{ATQ} or PLI_{CID} .

For each power level, the test report shall be as specified in 7.1.6.7.

7.1.9.4 PCD EMD immunity test

The steps b) to l) of the procedure specified in 7.1.8.2 shall be repeated for every power level between minimum and maximum power level obtained by PLI_{ATQ} or PLI_{CID} .

For each power level, the test report shall be as specified in 7.1.8.3.

"

Page 38, 7.2.1.1

Replace the text with the following:

"The purpose of this test is to verify that the load modulation amplitude V_{LMA} of the PICC and the phase parameters $\emptyset_{\text{LM, INTER}}$ and $\emptyset_{\text{LM, INTRA}}$ of the PICC conform to ISO/IEC 14443-2 for all mandatory and supported optional PICC to PCD bit rates within the operating field range [H_{min} respectively H_{LP} if the PICC supports PLI_{ATQ} or PLI_{CID} , H_{max}]."

Page 40, 7.2.2.1

Replace the text with the following:

"The purpose of this test is to determine that the PICC does not generate an electromagnetic disturbance amplitude V_{EMD} higher than $V_{\text{E, PICC}}$ during $t_{\text{E, PICC}}$ with the exceptions defined in ISO/IEC 14443-2 within the operating field range [H_{min} respectively H_{LP} if the PICC supports PLI_{ATQ} or PLI_{CID} , H_{max}] as specified in ISO/IEC 14443-2 for all supported PICC to PCD bit rates.

NOTE 1 The low EMD time $t_{\text{E, PICC}}$ is a function of FDT/TR0 as defined in ISO/IEC 14443-3:2018, 8.2.

NOTE 2 The EMD limit $V_{\text{E, PICC}}$ is a function of the field strength.

"

Page 41, 7.2.3.1

Replace the text with the following:

"The purpose of this test is to verify the ability of the PICC to receive the PCD commands within the operating field range [H_{min} respectively H_{LP} if the PICC supports PLI_{ATQ} or PLI_{CID} , H_{max}] as specified in ISO/IEC 14443-2 for all supported PCD to PICC bit rates."

Page 45, 7.2.5.1

Replace the text with the following:

"This test is used to measure the PICC loading effect at the minimum operating field strength H_{min} respectively H_{LP} if the PICC supports PLI_{ATQ} or PLI_{CID} as specified in ISO/IEC 14443-2."

Page 45, 7.2.5.2

Add the following paragraph after the 3rd paragraph:

"If the PICC supports PLI_{ATQ} or PLI_{CID} , the test shall be repeated at a field strength of H_{LP} , with the Reference PICC having R2 value, or alternatively the applied voltage on CON2, set for a field strength of H_{LP} ."

Page 46, 7.2.6.1

Replace the text with the following:

"This test verifies that the PICC operates as intended within the operating field range [H_{min} respectively H_{LP} if the PICC supports PLI_{ATQ} or PLI_{CID} , H_{max}] as specified in ISO/IEC 14443-2 for all supported PCD to PICC bit rates."

Page 47, 7.2.7

Add the following subclause after 7.2.6.4:

"

7.2.7 Procedures for PICC supporting optional PLI_{ATQ} or PLI_{CID} values

7.2.7.1 Scope

These tests apply only to PICCs which support PLI_{ATQ} or PLI_{CID} values.

If the PICC supports optional PLI_{ATQ} or PLI_{CID} values, the additional procedures specified in 7.2.1, 7.2.2, 7.2.3, 7.2.5 and 7.2.6 and the additional procedures specified in 7.2.7.2 to 7.2.7.4 shall be used to verify that:

- a) the PICC complies with the requirements specified in ISO/IEC 14443-2:2020/Amd 1, ISO/IEC 14443-3:2018/Amd 1 and ISO/IEC 14443-4:2018/Amd 1;
- b) the PICC complies with the transmission requirements specified in ISO/IEC 14443-2 for a field strength of H_{LP} ;
- c) the PICC complies with the EMD level and low EMD time requirements specified in ISO/IEC 14443-2 and ISO/IEC 14443-3 for a field strength of H_{LP} ;
- d) the PICC complies with the reception requirements specified in ISO/IEC 14443-2 for a field strength of H_{LP} ;
- e) the PICC complies with the maximum loading effect requirements specified in 7.2.5 for a field strength of H_{LP} ;
- f) the PICC complies with operating field strength requirements specified in 7.2.6 for a field strength of H_{LP} .

7.2.7.2 Determination of PICC minimum requested field strength H_{LP}

The following sequence is applied to determine the minimum field strength H_{LP} that the PICC may request and at which it shall comply with all ISO/IEC 14443 requirements.

- a) Find the minimum field strength at which the PICC still indicates that its received field strength is at least ($H_{LP} + H_{step, max}$), with a resolution of 0,1 dB (a factor of $\sim 1,012$). $H_{step, max}$ is specified in ISO/IEC 14443-2:2020/Amd 1:2021, 6.3.

NOTE This can be achieved by decreasing the Test PCD assembly field strength by steps of 0,1 dB while the PICC indicates its received field strength is at least $(H_{LP} + H_{step, max})$ or by using a dichotomic search.

- b) Obtain H_{LP} by subtracting $H_{step, max}$ to the minimum field strength at which the PICC still indicates that its received field strength is at least $(H_{LP} + H_{step, max})$.

7.2.7.3 Maximum field strength change test using PLI_{ATQ}

7.2.7.3.1 General

This subclause verifies PICC operation after worst case field strength steps following PLI_{ATQ} indication.

7.2.7.3.2 Procedure

Perform the following steps for single step up:

- a) Adjust the RF power delivered by the signal generator to the Test PCD antenna to produce the PICC minimum requested field strength H_{LP} as measured by the calibration coil.
- b) Place the PICC under test into the DUT position. The RF drive into the Test PCD antenna shall be readjusted to the required field strength if necessary.
- c) Send a REQA for PICC Type A or a REQB(AFI, N=1) for PICC Type B.
- d) If PLI_{ATQ} in the PICC response is not (00)b then send a step increase of $H_{step, max}$ to the Test PCD assembly power amplifier to set the Test PCD assembly field strength with minimum achievable rise/fall time.
- e) Immediately after a guard time of t_{PL} (as specified in ISO/IEC 14443-3:2018/Amd 1:2021, 6.5.2.3), send start of communication or SOF of the next anticollision command, AC for PICC Type A or ATTRIB(PUPI) for PICC Type B.
- f) Check that the PICC response is as expected.
- g) Put the PICC in IDLE state by sending a REQA for PICC Type A or a DESELECT and a WUPB(nAFI) for PICC Type B.

NOTE 1 If the PICC Type B is not compliant with ISO/IEC 14443-4, then commands used in steps e) and g) can be modified, e.g. using HLTB(PUPI) in step e) and WUPB(nAFI) in step g).

- h) Repeat steps c) to g) until the Test PCD assembly field strength is H_{max} , using a smaller value for the last step increase if necessary, or until PLI_{ATQ} is (00)b at step d).

Perform the following steps for single step down:

- i) Adjust the RF power delivered by the signal generator to the Test PCD antenna to produce the PICC maximum field strength H_{max} as measured by the calibration coil.
- j) Send a REQA for PICC Type A or a REQB(AFI, N=1) for PICC Type B.
- k) If PLI_{ATQ} is (11)b then send a step decrease of $H_{step, max}$ to the Test PCD assembly power amplifier to set the Test PCD assembly field strength with minimum achievable rise/fall time.
- l) Immediately after a guard time of t_{PL} , send start of communication or SOF of the next anticollision command, AC for PICC Type A or ATTRIB(PUPI) for PICC Type B.
- m) Check that the PICC response is as expected.
- n) Put the PICC in IDLE state by sending a REQA for PICC Type A or a DESELECT and a WUPB(nAFI) for PICC Type B.

NOTE 2 If the PICC Type B is not compliant with ISO/IEC 14443-4, then commands used in steps l) and n) can be modified, e.g. using HLTB(PUPI) in step l) and WUPB(nAFI) in step n).

o) Repeat steps j) to n) until PLI_{ATQ} is not (11)b at step k).

Perform the following steps for multiple step up:

p) Adjust the RF power delivered by the signal generator to the Test PCD antenna to produce the PICC minimum requested field strength H_{LP} as measured by the calibration coil.

q) Send a REQA for PICC Type A or a REQB(AFI, N=1) for PICC Type B.

r) If PLI_{ATQ} is not (00)b then send several consecutive steps increase of $H_{step, max}$ to the Test PCD assembly power amplifier to set the Test PCD assembly field strength with minimum achievable rise/fall time, each step increase being followed by a guard time of t_{PL} , up to a field strength of H_{max} as measured by the calibration coil.

NOTE 3 The last step increase can have a smaller value to reach exactly H_{max} .

s) Immediately after the last guard time of t_{PL} , send start of communication or SOF of the next anticollision command, AC for PICC Type A or ATTRIB(PUPI) for PICC Type B.

t) Check that the PICC response is as expected.

NOTE 4 In any step of this procedure, t_{PL} can be set to a non-default value by PLI_{ATQ} . This new current value applies until a subsequent setting or until the end of the procedure as the PICC is never reset to POWER-OFF state during the procedure.

7.2.7.3.3 Test report

The test is PASS if the PICC response in steps f), m) and t) is as expected, otherwise the test is FAIL.

7.2.7.4 Maximum field strength change test using PLI_{CID}

7.2.7.4.1 General

This subclause verifies PICC operation after worst case field strength steps following PLI_{CID} indication.

7.2.7.4.2 Procedure

Perform the following steps for single step up:

a) Adjust the RF power delivered by the signal generator to the Test PCD antenna to produce the PICC minimum requested field strength H_{LP} as measured by the calibration coil.

b) Place the PICC under test into the DUT position. The RF drive into the Test PCD antenna shall be readjusted to the required field strength if necessary.

c) Put the PICC in PROTOCOL state and initiate a first I-block exchange.

d) If PLI_{CID} in the PICC response is not (00)b then send a step increase of $H_{step, max}$ to the Test PCD assembly power amplifier to set the Test PCD assembly field strength with minimum achievable rise/fall time.

e) Immediately after a guard time of t_{PL} (as specified in ISO/IEC 14443-4:2018/Amd 1:2021, 7.5), send start of communication or SOF of the next block.

f) Check that the PICC response is as expected.

g) Repeat steps d) to f) until the Test PCD assembly field strength is H_{max} , using a smaller value for the last step increase if necessary, or until PLI_{CID} is (00)b at step d).

Perform the following steps for single step down:

h) Adjust the RF power delivered by the signal generator to the Test PCD antenna to produce the PICC maximum field strength H_{max} as measured by the calibration coil.

- i) Initiate an I-block exchange.
- j) If PLI_{CID} is (10)b or (11)b then send a step decrease of $H_{step, max}$ to the Test PCD assembly power amplifier to set the Test PCD assembly field strength with minimum achievable rise/fall time.
- k) Immediately after a guard time of t_{PL} , send start of communication or SOF of the next block.
- l) Check that the PICC response is as expected.
- m) Repeat steps j) to l) until PLI_{CID} is neither (10)b nor (11)b at step j).

Perform the following steps for multiple step up:

- n) Adjust the RF power delivered by the signal generator to the Test PCD antenna to produce the PICC minimum requested field strength H_{LP} as measured by the calibration coil.
- o) Initiate an I-block exchange.
- p) If PLI_{CID} is not (00)b then send several consecutive steps increase of $H_{step, max}$ to the Test PCD assembly power amplifier to set the Test PCD assembly field strength with minimum achievable rise/fall time, each step increase being followed by a guard time of t_{PL} , up to a field strength of H_{max} as measured by the calibration coil.

NOTE 1 The last step increase can have a smaller value to reach exactly H_{max} .

- q) Immediately after the last guard time of t_{PL} , send start of communication or SOF of the next block.
- r) Check that the PICC response is as expected.

NOTE 2 In any step of this procedure, t_{PL} can be set to a non-default value by PLI_{ATQ} or by S(WTX). This new current value applies until a subsequent setting or until the end of the procedure as the PICC is never reset to POWER-OFF state during the procedure.

7.2.7.4.3 Test report

The test is PASS if the PICC response in steps f), l) and r) is as expected, otherwise the test is FAIL.

"

Page 240, H.5

Add the following subclause after H.4.5.4 and renumber the subsequent subclauses and tables:

"

H.5 Handling of PLI_{ATQ} or PLI_{CID}

H.5.1 General

The purpose of this test is to determine the handling of PLI_{ATQ} or PLI_{CID} according to ISO/IEC 14443-3:2018/Amd 1:2021, 6.5.2.3 and ISO/IEC 14443-4:2018/Amd 1:2021, 7.5. This test shall be executed with reference PICCs corresponding to all mandatory and optionally supported classes.

H.5.2 Apparatus

See H.1.

H.5.3 Procedure

Place the LT into the PCD operating volume and record the presence and the content of the PCD commands.